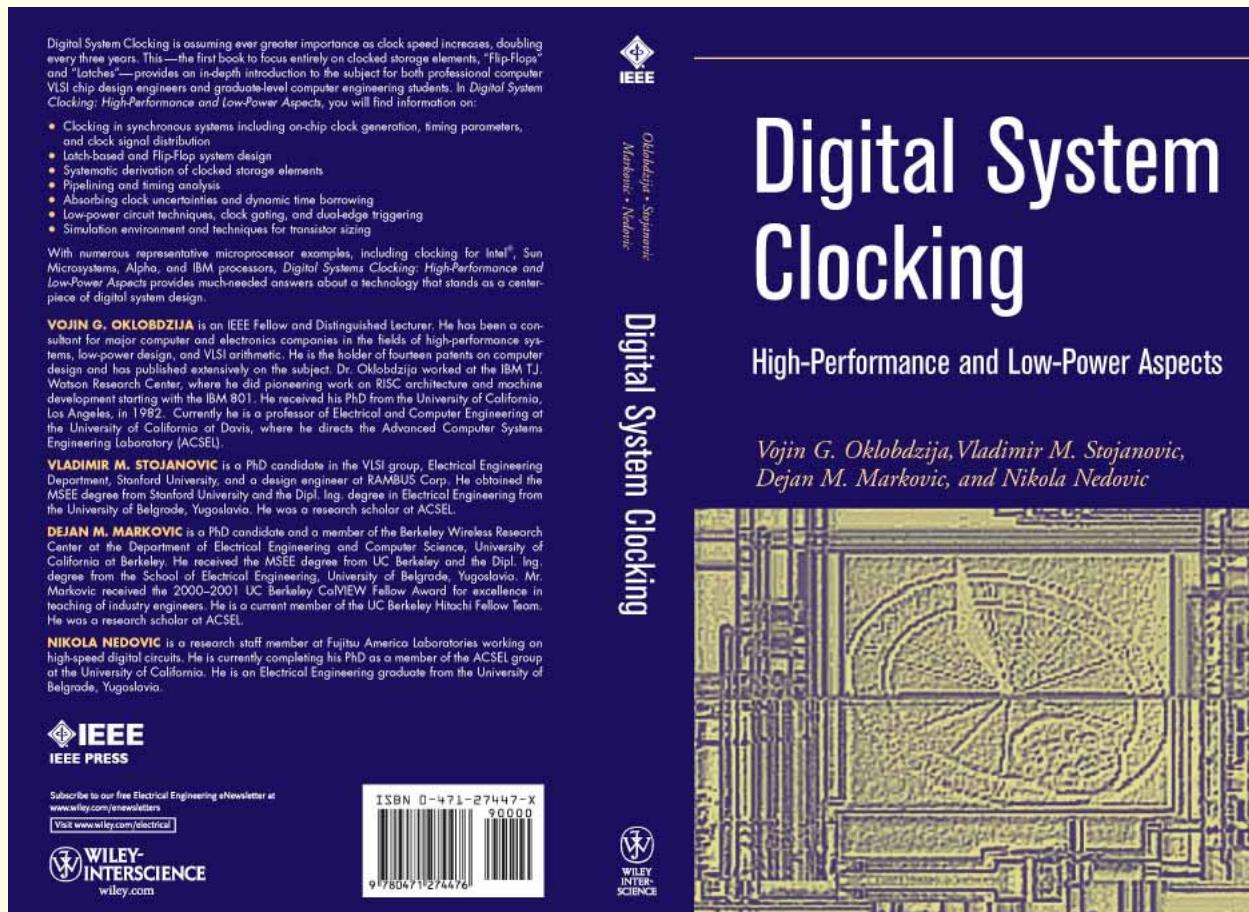


Digital System Clocking: *High-Performance and Low-Power Aspects*

Vojin G. Oklobdzija, Vladimir M. Stojanovic, Dejan M. Markovic, Nikola M. Nedovic



Digital System Clocking is assuming ever greater importance as clock speed increases, doubling every three years. This—the first book to focus entirely on clocked storage elements, “Flip-Flops” and “Latches”—provides an in-depth introduction to the subject for both professional computer VLSI chip design engineers and graduate-level computer engineering students. In Digital System Clocking: High-Performance and Low-Power Aspects, you will find information on:

- Clocking in synchronous systems including on-chip clock generation, timing parameters, and clock signal distribution
- Latch-based and Flip-Flop system design
- Systematic derivation of clocked storage elements
- Pipelining and timing analysis
- Absorbing clock uncertainties and dynamic time borrowing
- Low-power circuit techniques, clock gating, and dual-edge triggering
- Simulation environment and techniques for transistor sizing

With numerous representative microprocessor examples, including clocking for Intel®, Sun Microsystems, Alpha, and IBM processors, *Digital Systems Clocking: High-Performance and Low-Power Aspects* provides much-needed answers about a technology that stands as a centerpiece of digital system design.

VOJIN G. OKLOBDZIJA is an IEEE Fellow and Distinguished Lecturer. He has been a consultant for major computer and electronics companies in the fields of high-performance systems, low-power design, and VLSI arithmetic. He is the holder of fourteen patents on computer design and has published extensively on the subject. Dr. Oklobdzija worked at the IBM T.J. Watson Research Center, where he did pioneering work on RISC architecture and machine development starting with the IBM 801. He received his PhD from the University of California, Los Angeles, in 1982. Currently he is a professor of Electrical and Computer Engineering at the University of California at Davis, where he directs the Advanced Computer Systems Engineering Laboratory (ACSEL).

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NIKOLA NEDOVIC is a research staff member at Fujitsu America Laboratories working on high-speed digital circuits. He is currently completing his PhD as a member of the ACSEL group at the University of California. He is an Electrical Engineering graduate from the University of Belgrade, Yugoslavia.



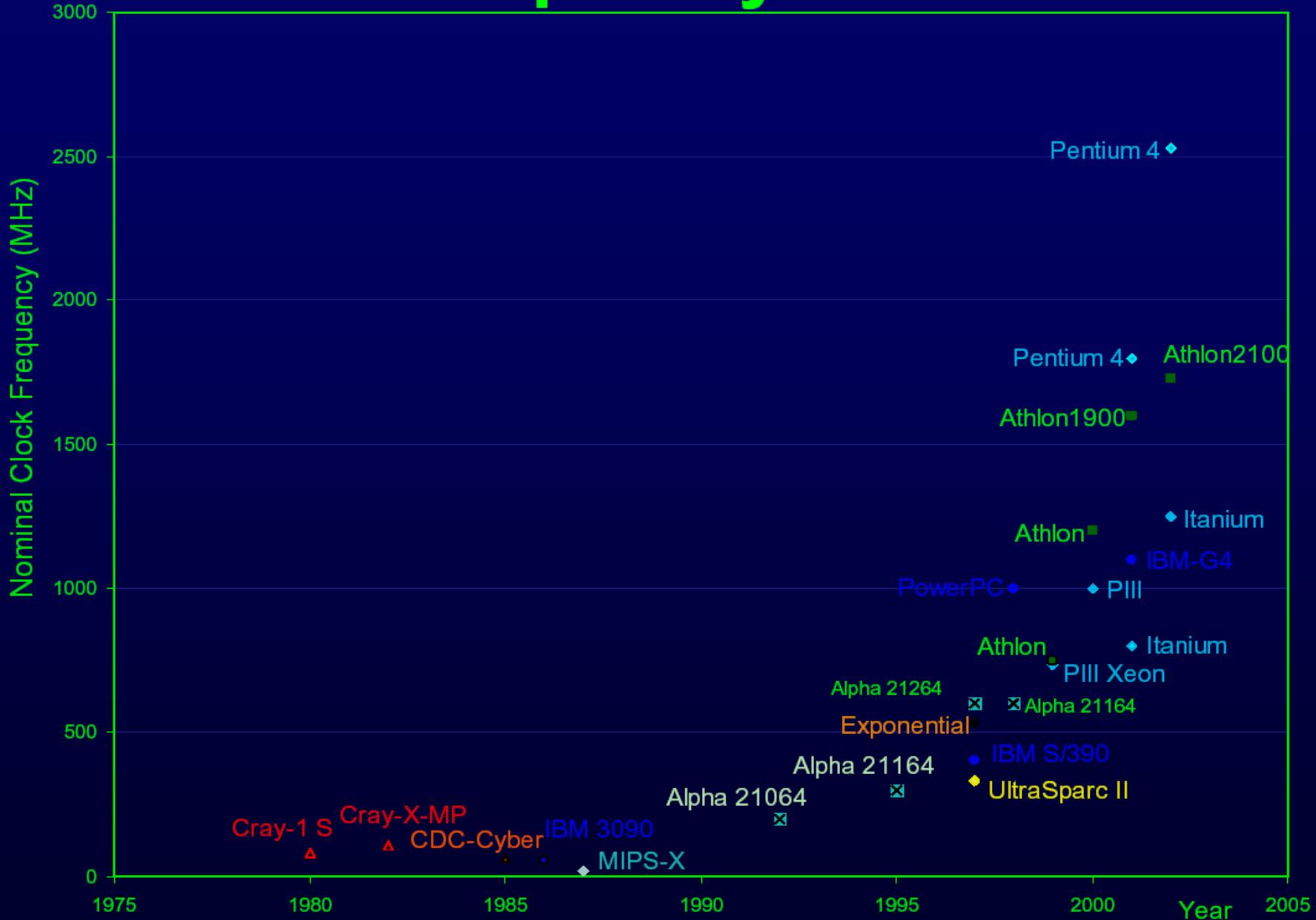
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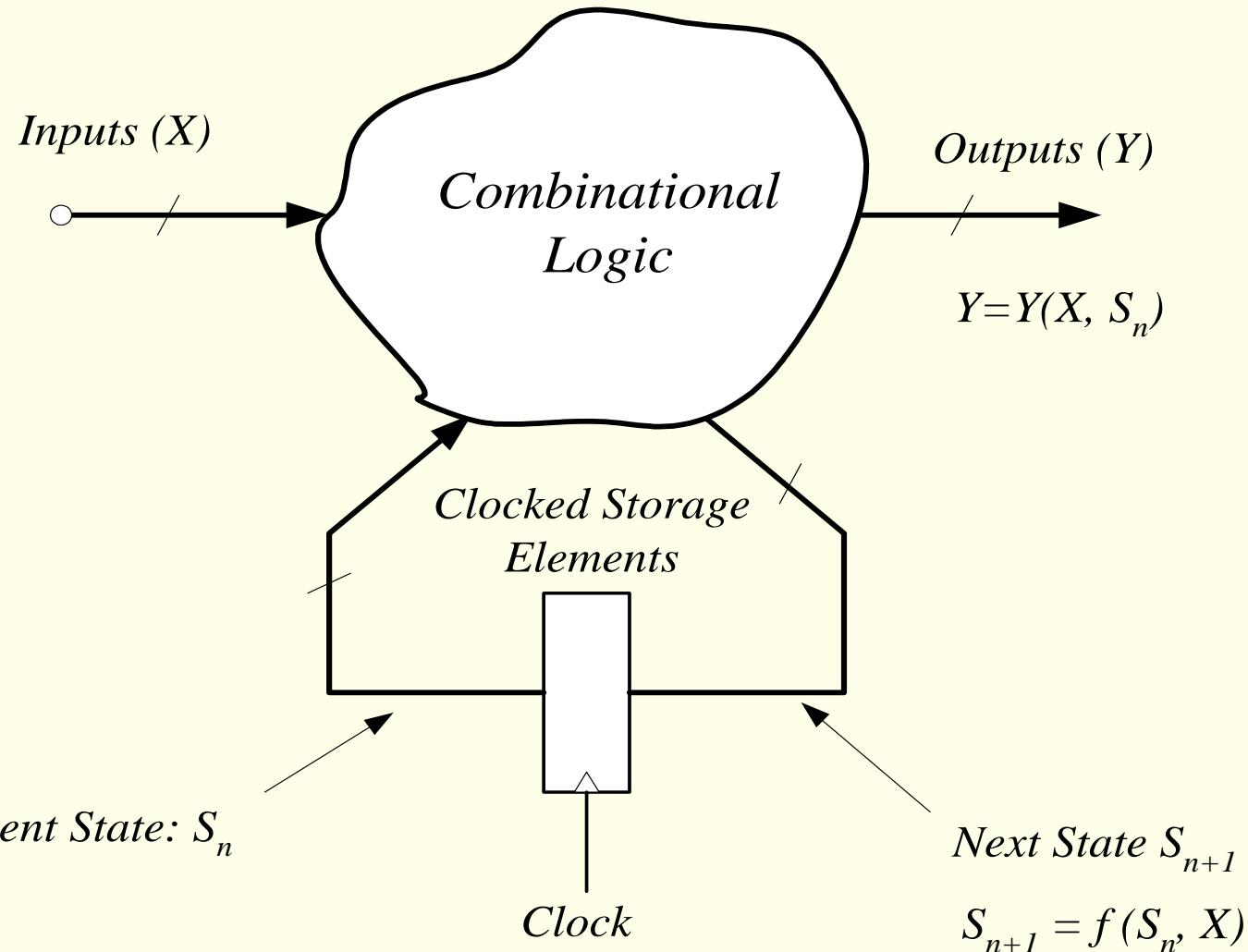
Clock frequency trends



Clock Frequency of Selected Historic Computers and Supercomputers

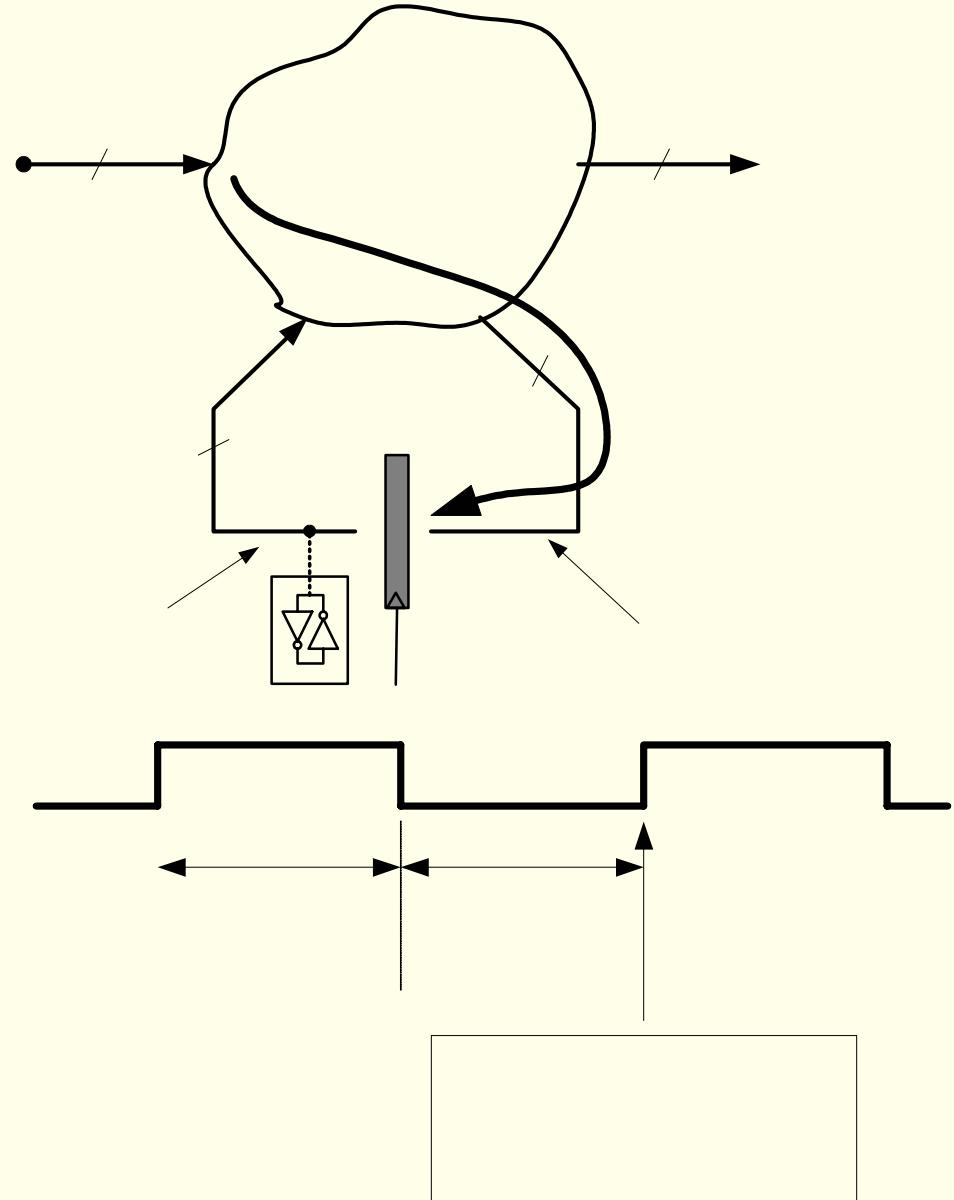
System	Intro Date	Technology	Class	Nominal Clock Period (nS)	Nominal Clock Frequency (MHz)
Cray-X-MP	1982	MSI ECL	Vector Processor	9.5	105.3
Cray-1S,-1M	1980	MSI ECL	Vector Processor	12.5	80.0
CDC Cyber 180/990	1985	ECL	Mainframe	16.0	62.5
IBM 3090	1986	ECL	Mainframe	18.5	54.1
Amdahl 58	1982	LSI ECL	Mainframe	23.0	43.5
IBM 308X	1981	LSI TTL	Mainframe	24.5, 26.0	40.8,38.5
Univac 1100/90	1984	LSI ECL	Mainframe	30.0	33.3
MIPS-X	1987	VLSI CMOS	Microprocessor	50.0	20.0
HP-900	1982	VLSI CMOS	Micro-mainframe	55.6	18.0
Motorola 68020	1985	VLSI CMOS	Microprocessor	60.0	16.7
Bellmac-32A	1982	VLSI CMOS	Microprocessor	125.0	8.0

The concept of Finite-State Machine: FSM (Hoffman Model)



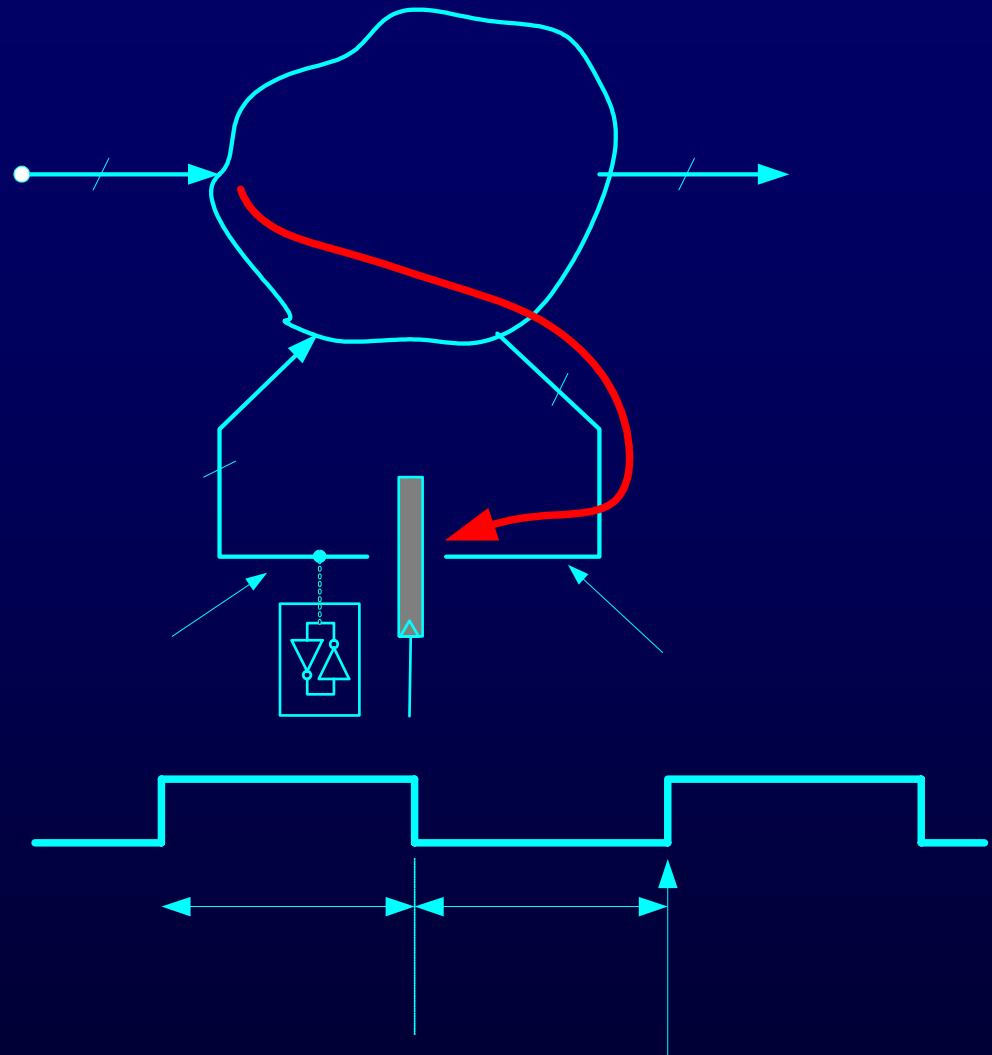
Another Representation of FSM

- Clocked Storage Elements: Flip-Flops and Latches should be viewed as **synchronization elements**, not merely as **storage elements** !
- Their main purpose is to **synchronize** fast and slow paths:
 - prevent the fast path from corrupting the state



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State Changes in the Finite-State Machine

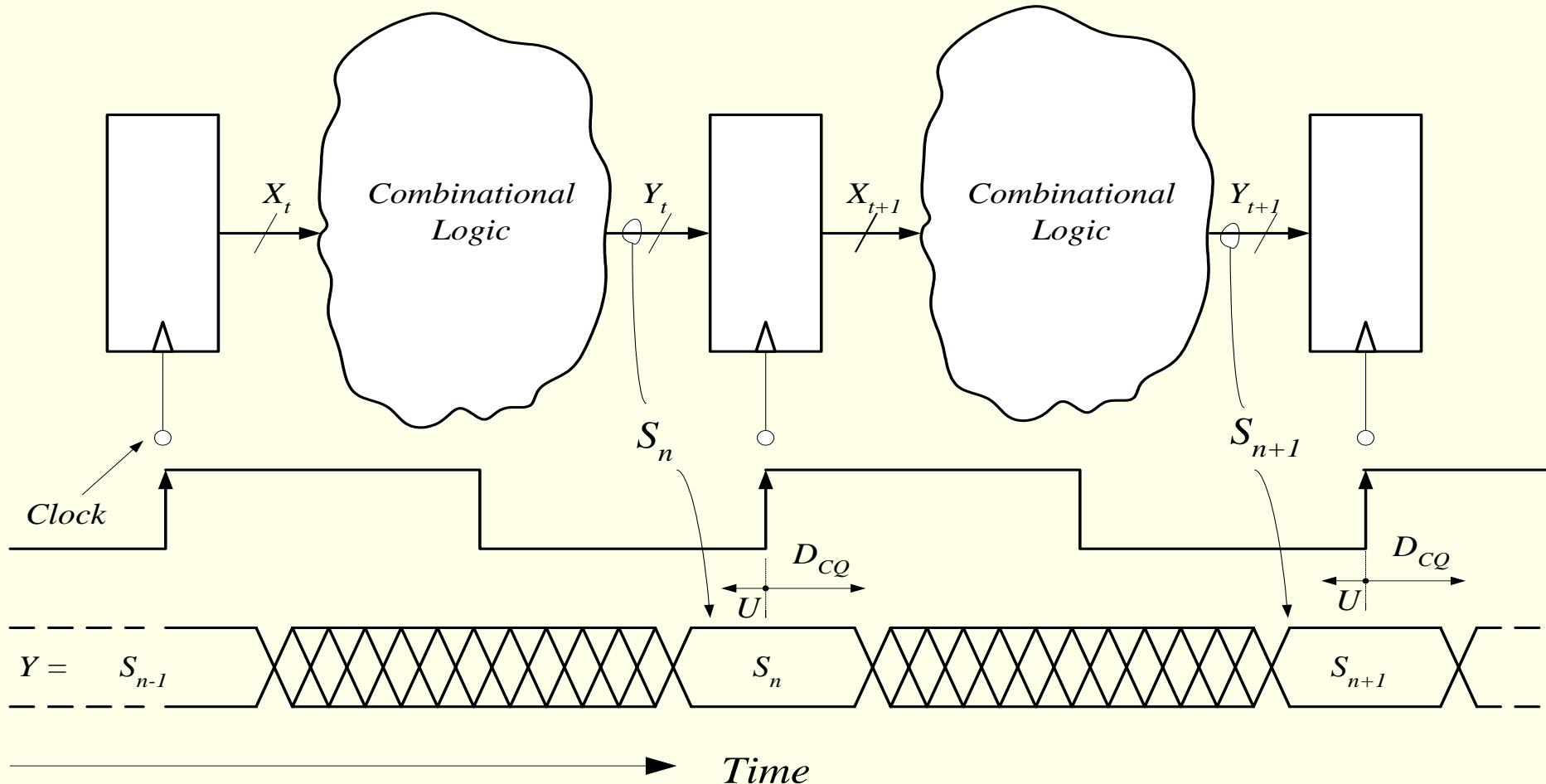
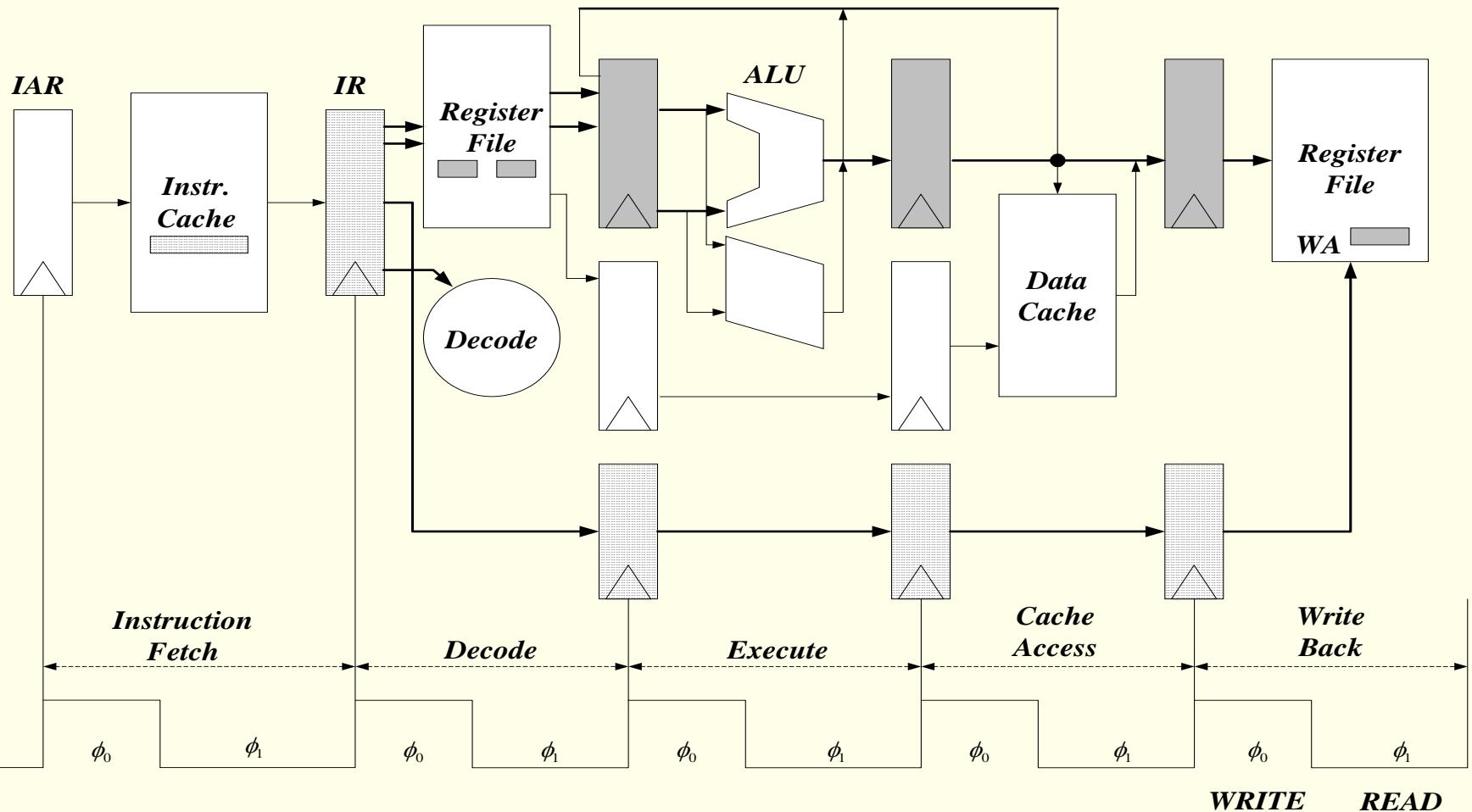
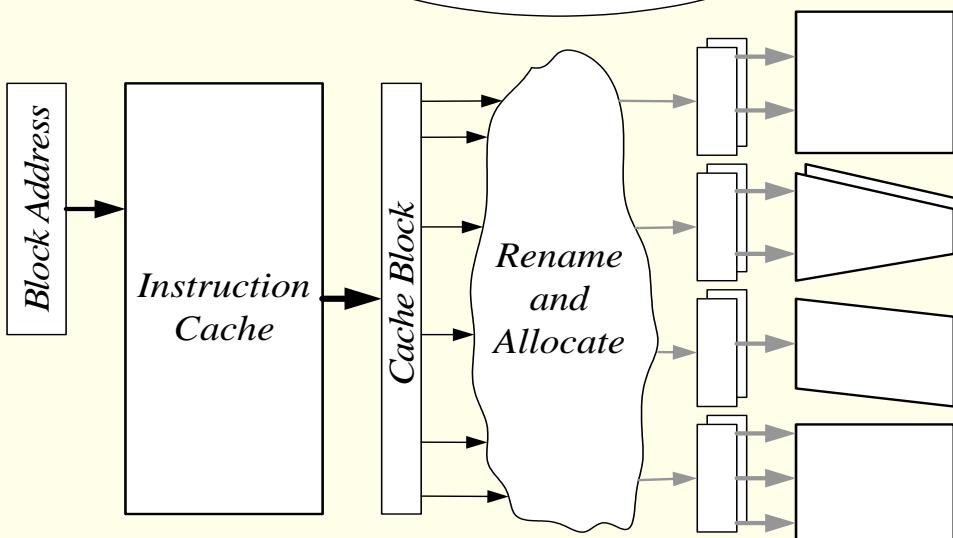
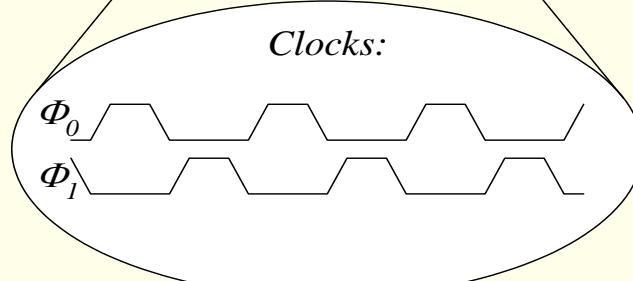
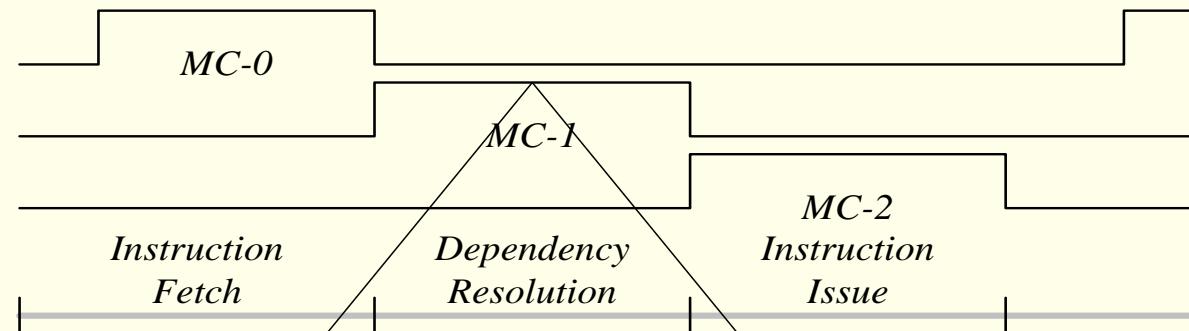


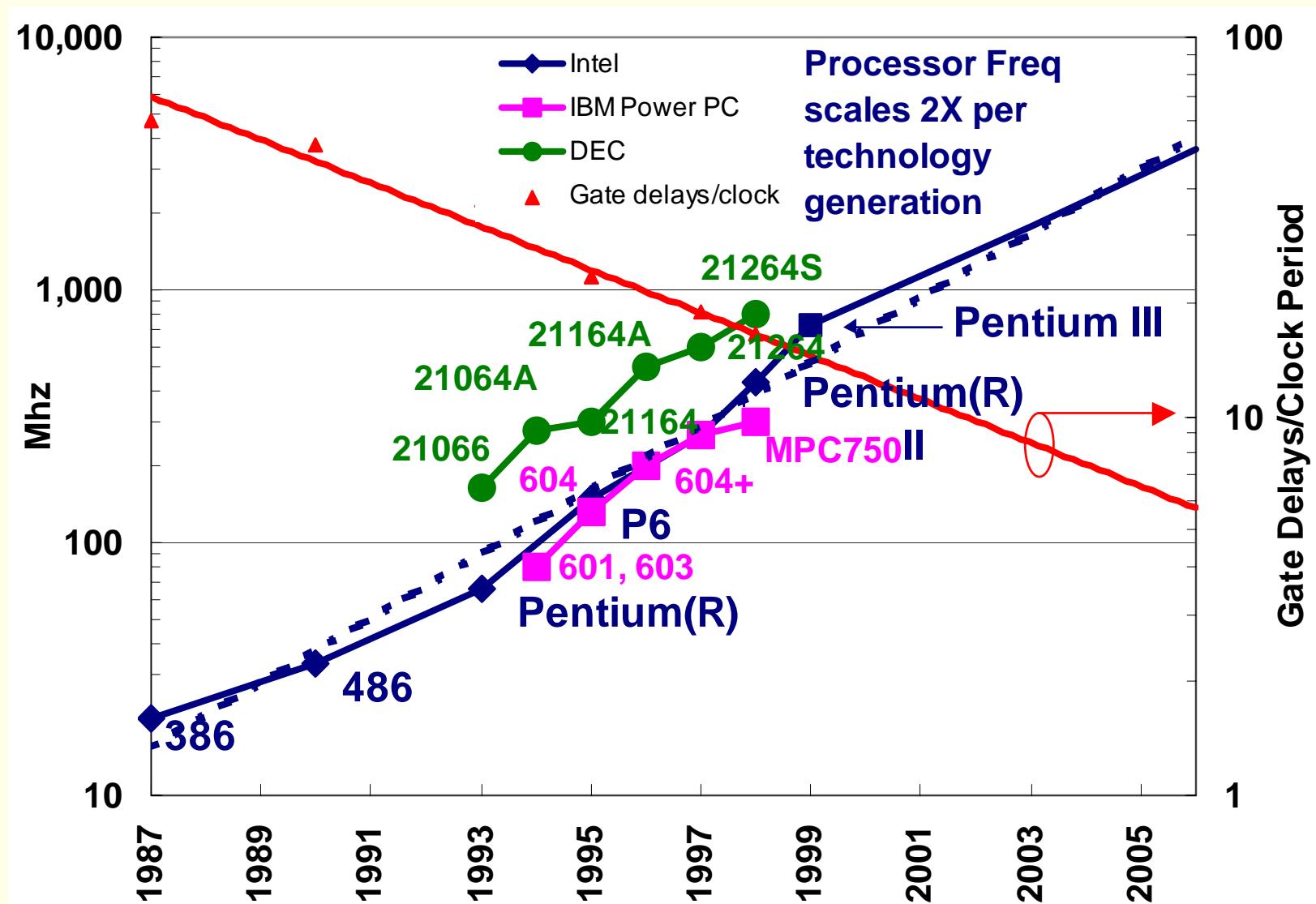
Diagram of a Pipelined System



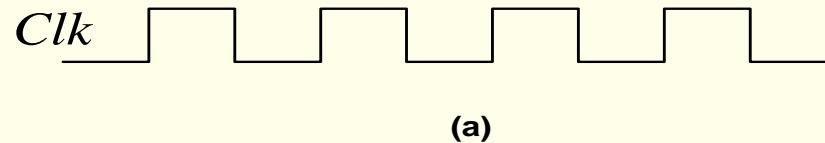
Machine Execution Phases with Respect to the Clock Cycles



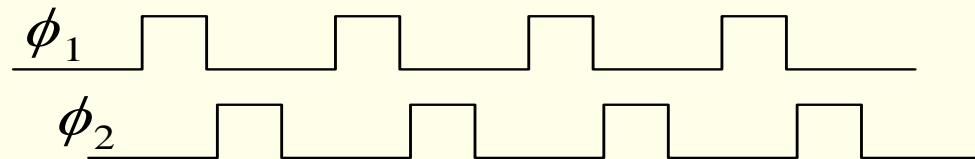
Increase in the Clock Frequency and Decrease in the Number of Logic Levels



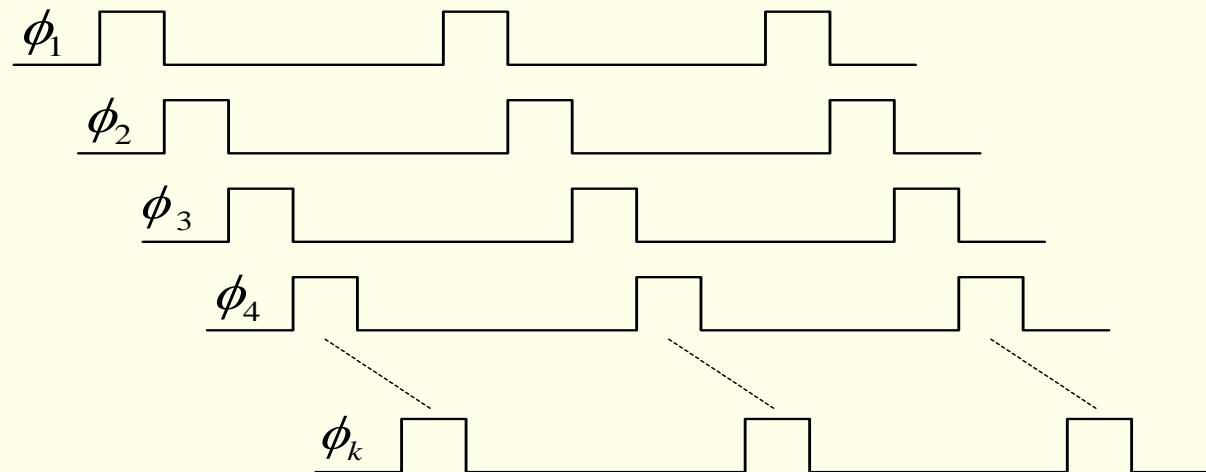
System clocking schemes: (a) single-phase clock; (b) two-phase clock; (c) multiple-phase clock



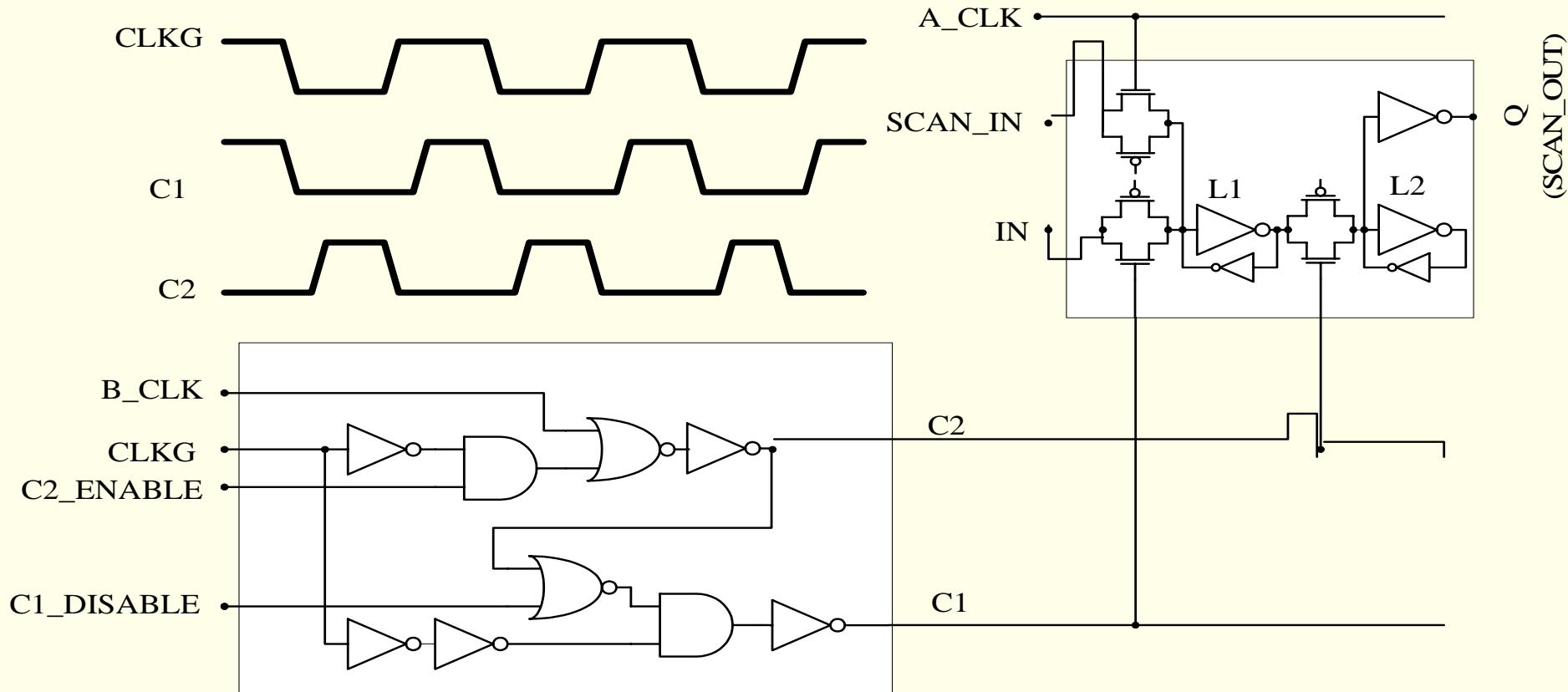
(a)

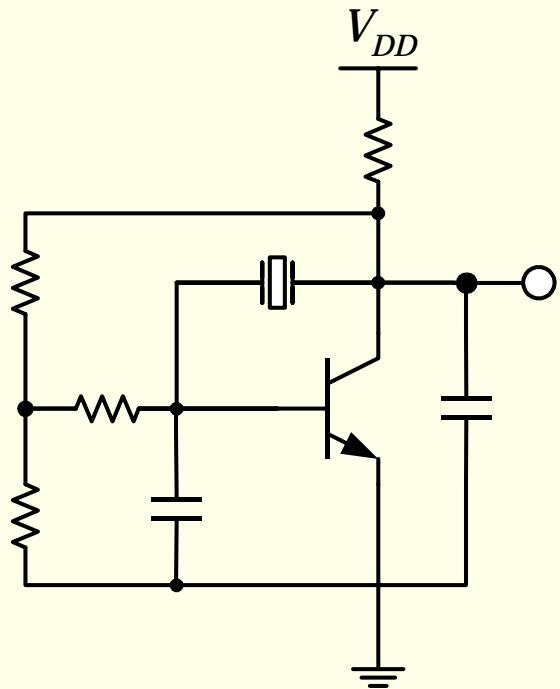


(b)



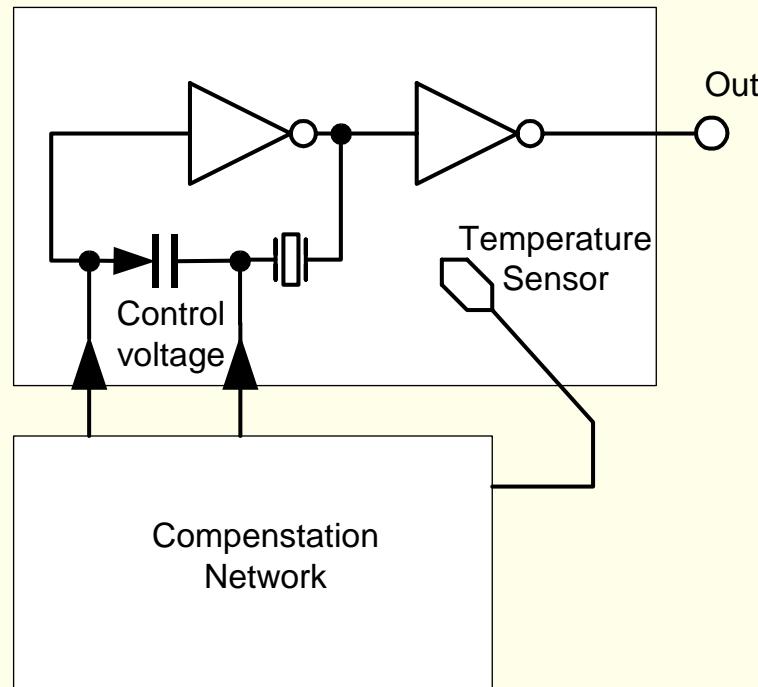
Local generation of Two-Phase Clocks as used in IBM S/390 G4





(a)

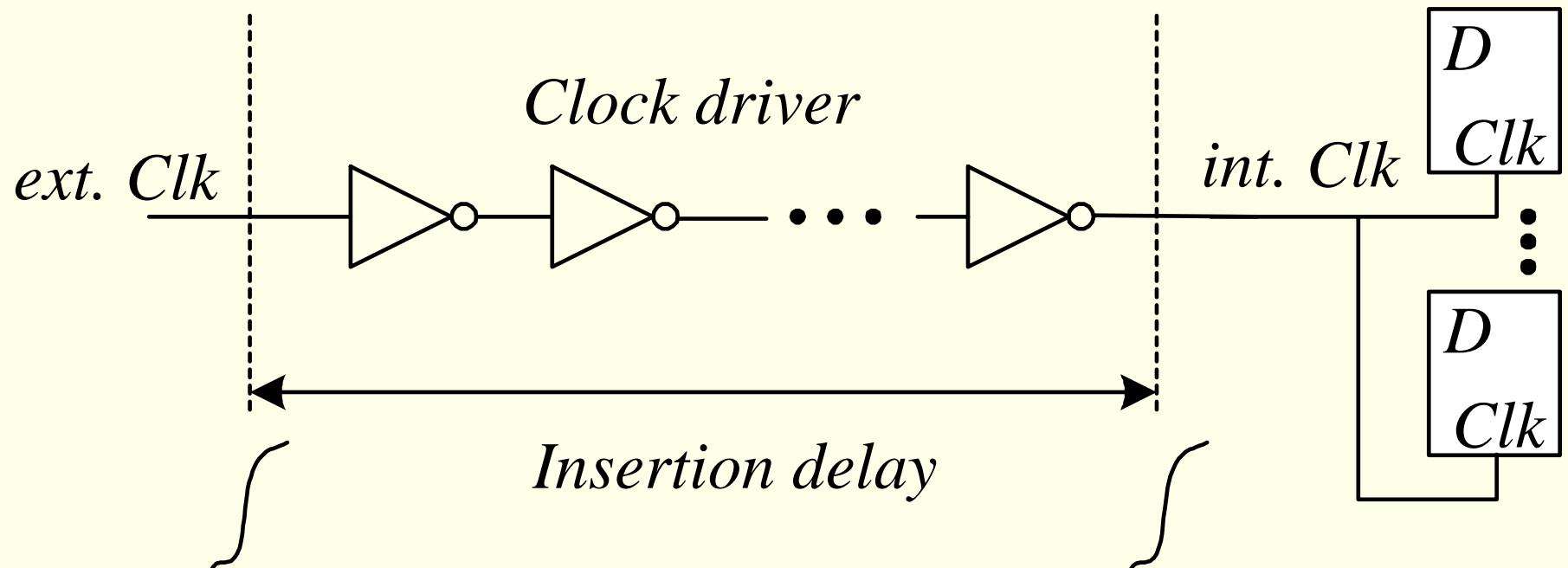
(a) Crystal oscillator



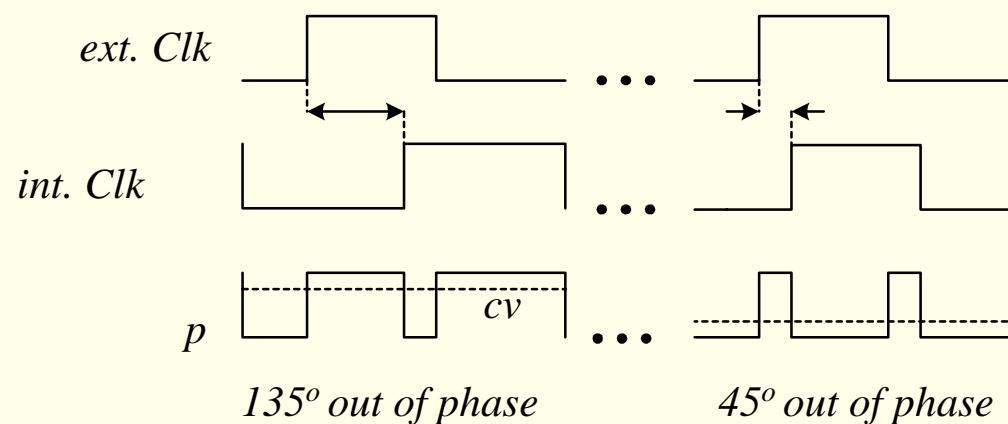
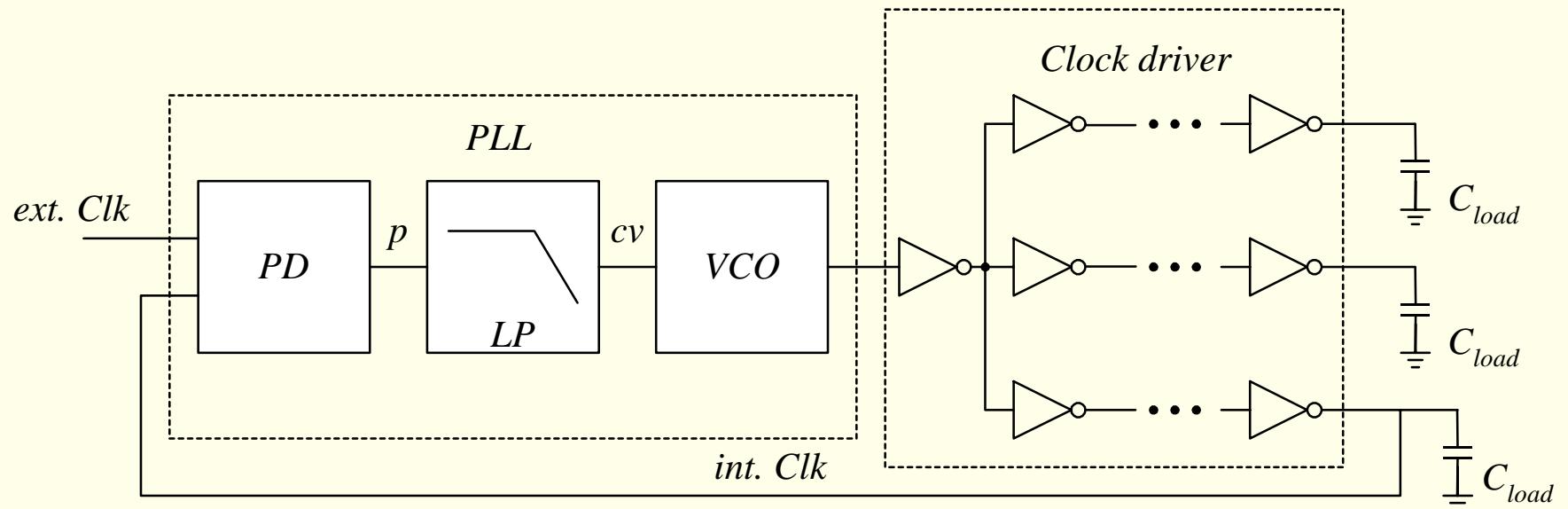
(b)

(b) Temperature-compensated crystal oscillator

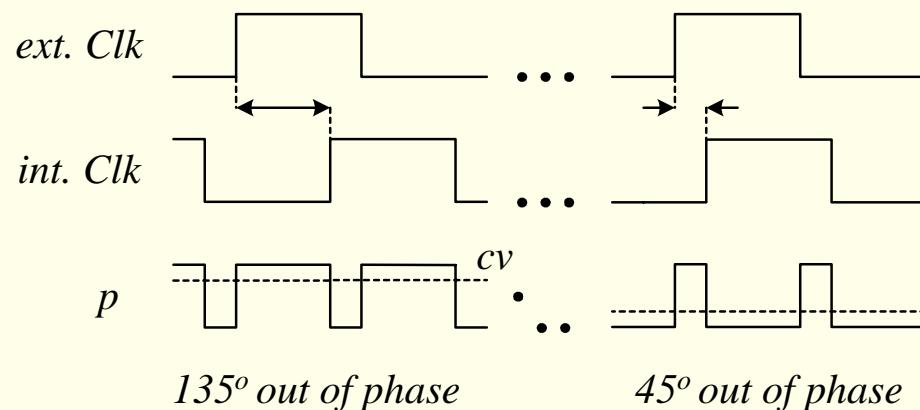
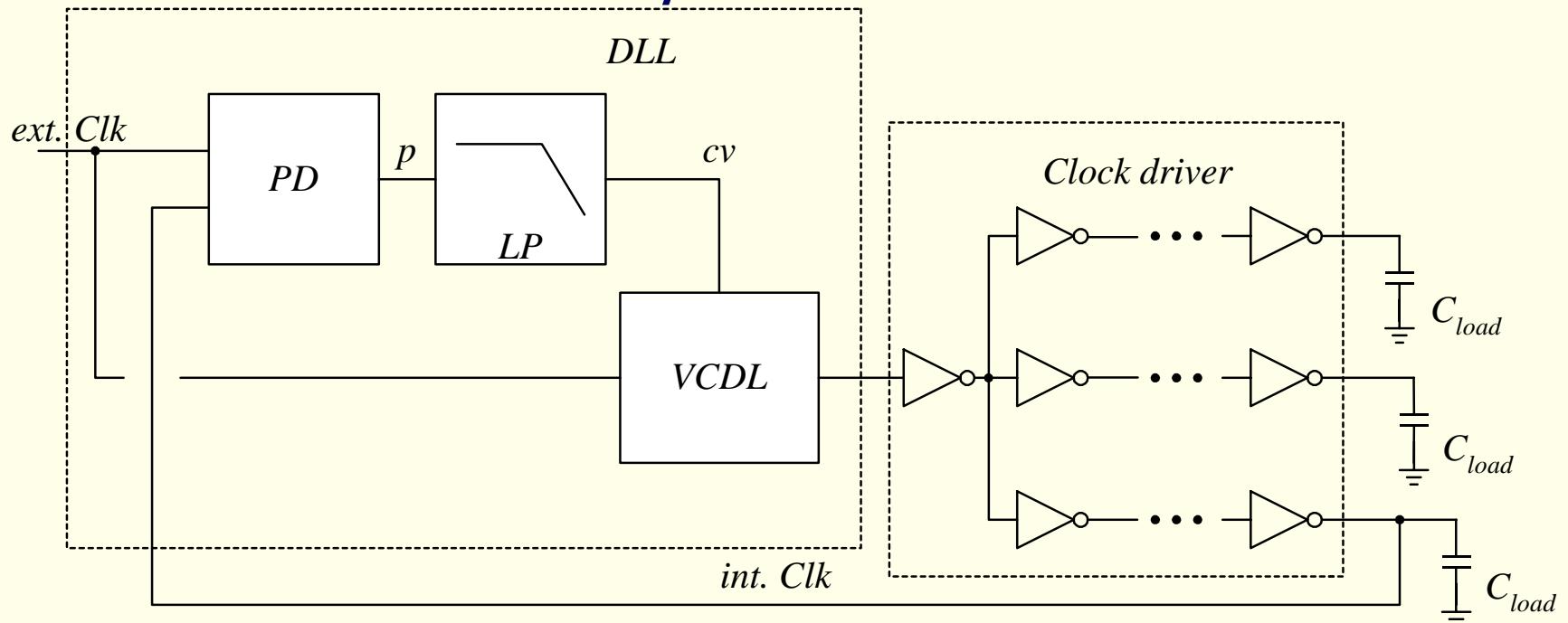
On-Chip Clock Insertion Delay



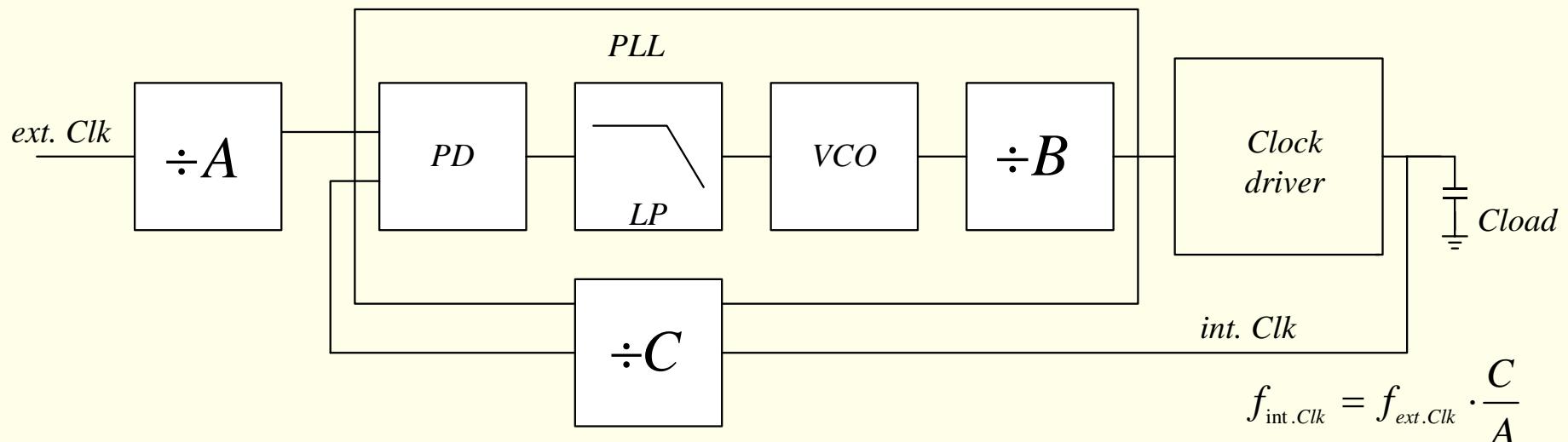
Phase-Locked Loop Block Diagram and Operation



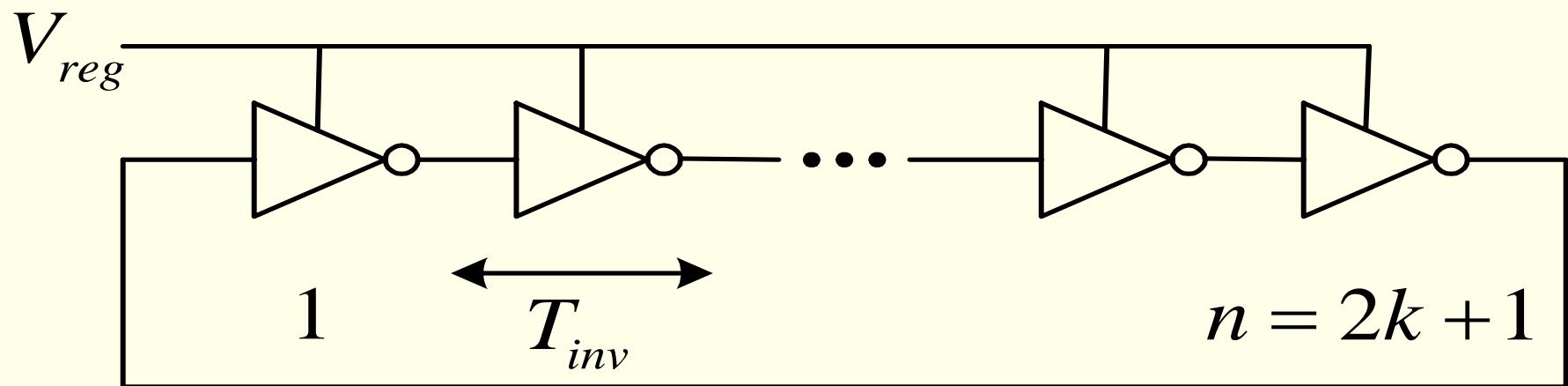
Delay-Locked Loop Block Diagram and Operation



PLL Frequency Multiplication

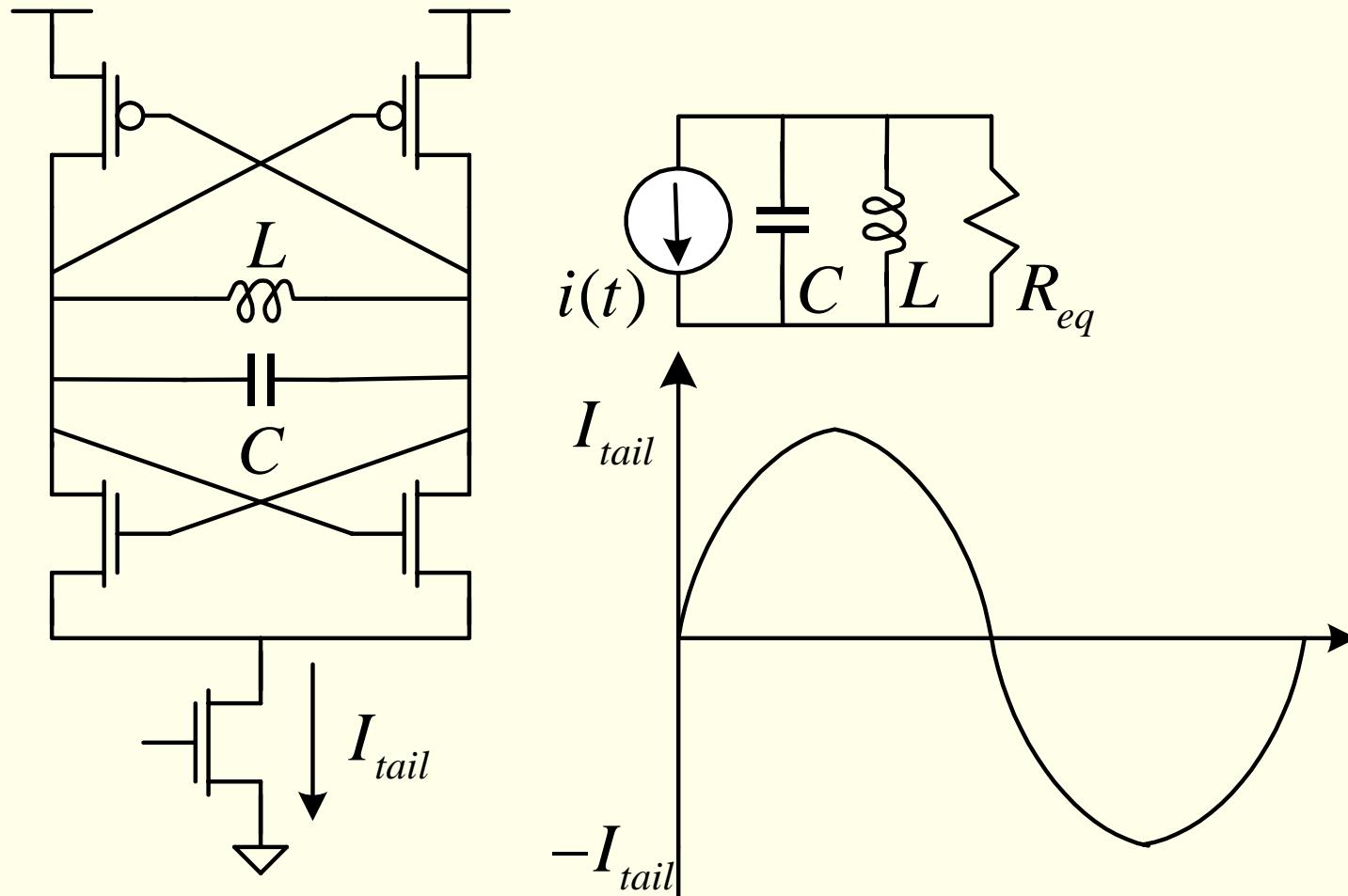


Ring-Oscillator-Based VCO with CMOS Inverters as Delay Elements

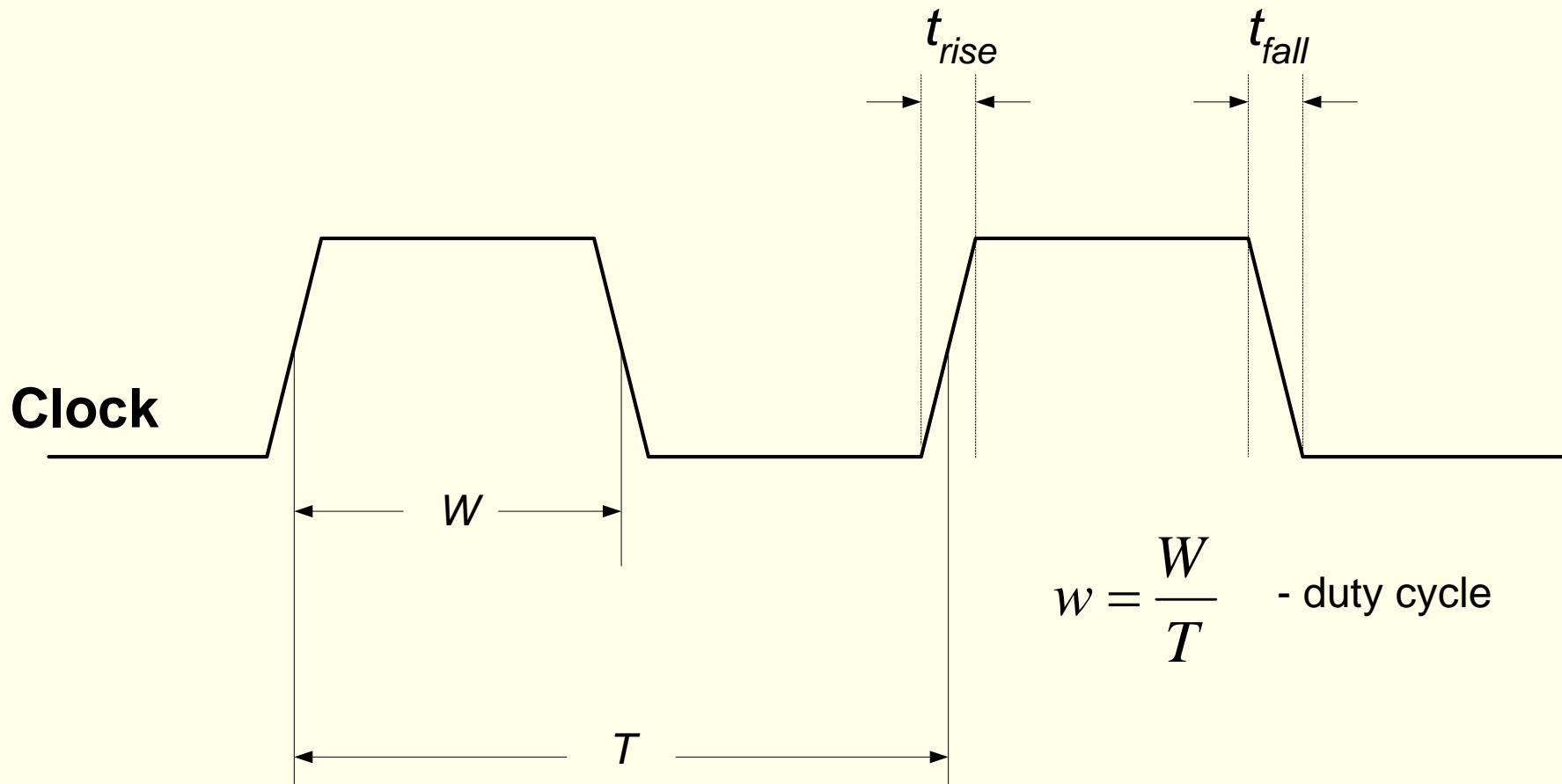


$$f_{osc} = \frac{1}{2nT_{inv}}; \quad k \geq 1$$

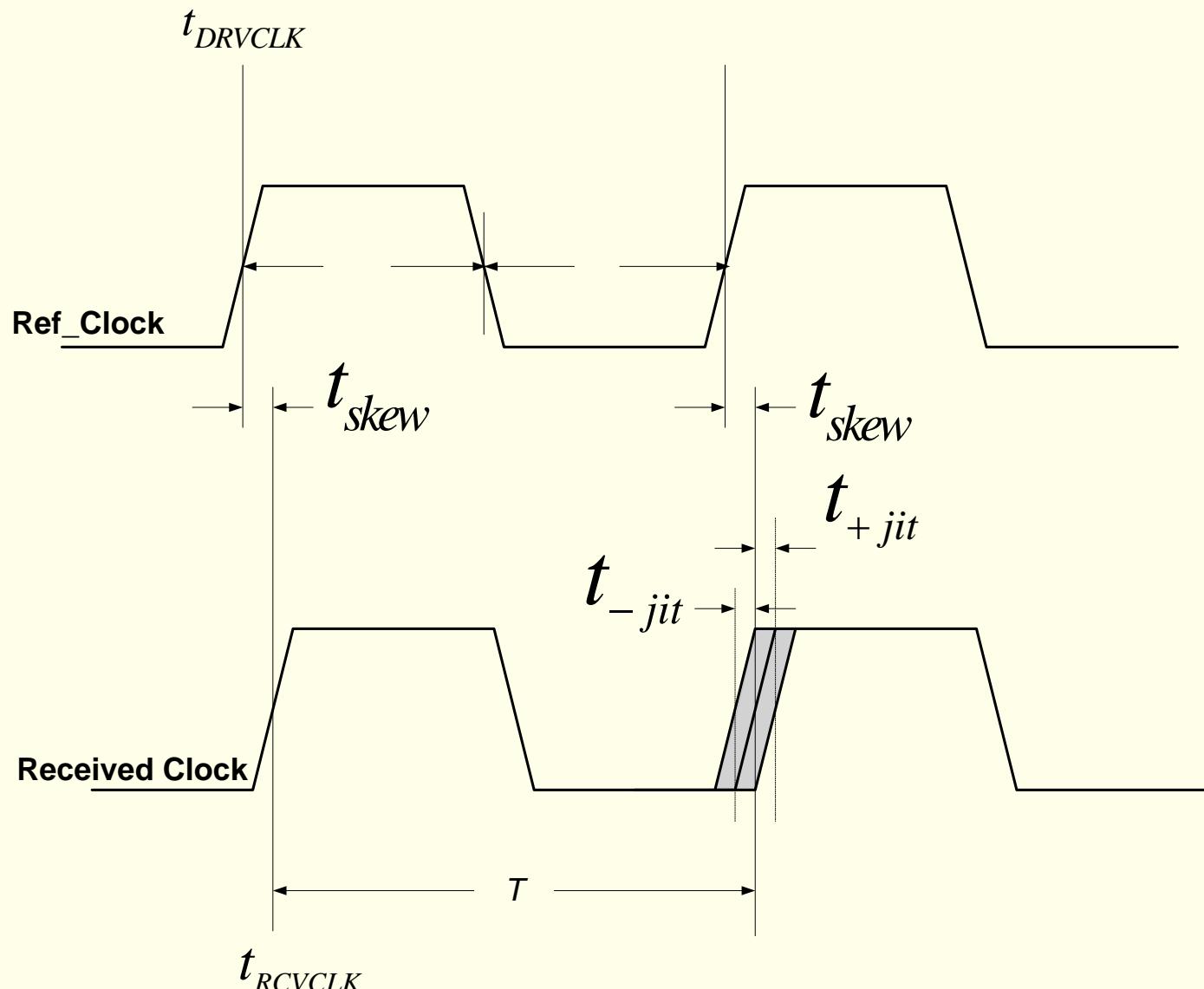
LC Tank-Based VCO, Equivalent AC Circuit Model and Current Waveform



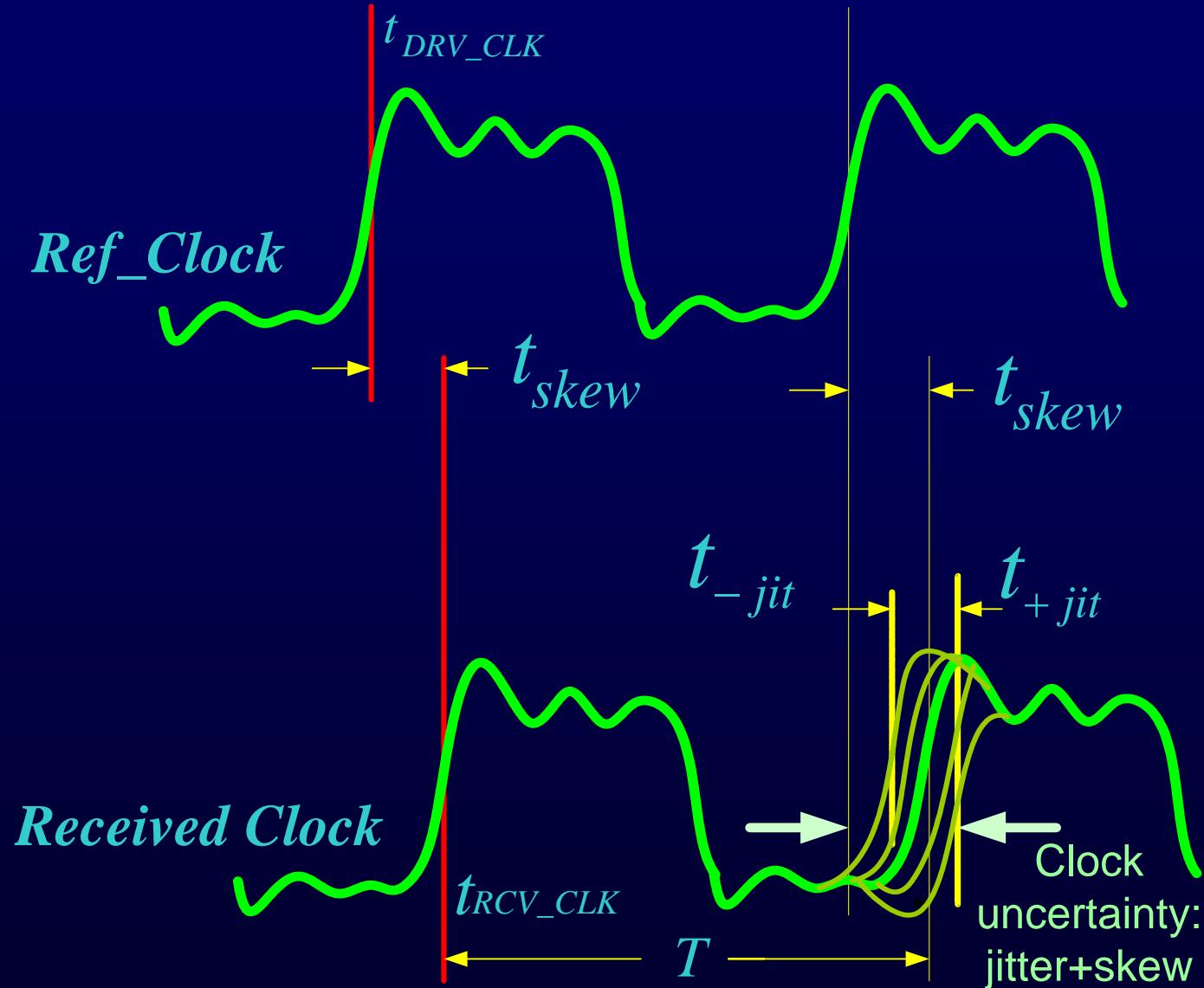
Clock Parameters: Period (T), Width, Rise and Fall Times



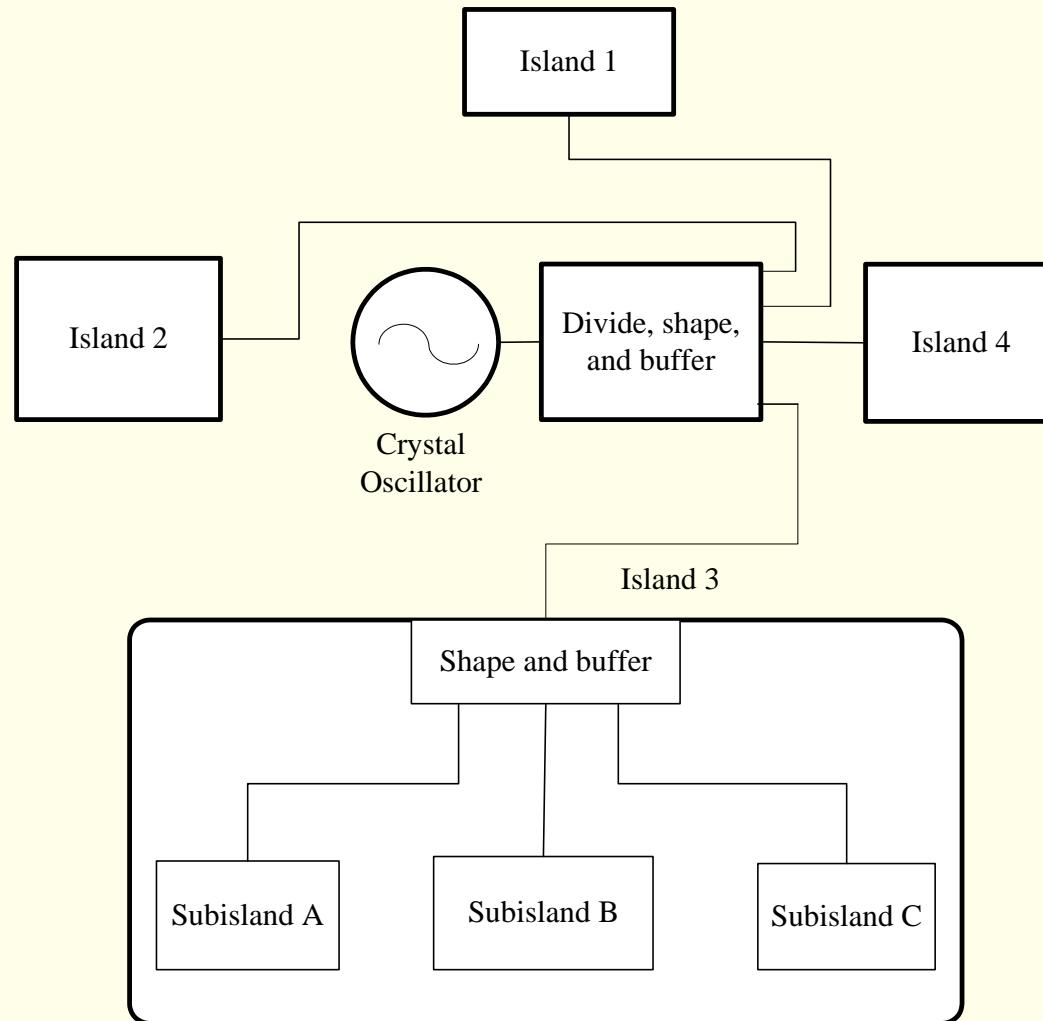
Clock Parameters: Period, Width, Clock Skew and Clock Jitter



Clock Uncertainties

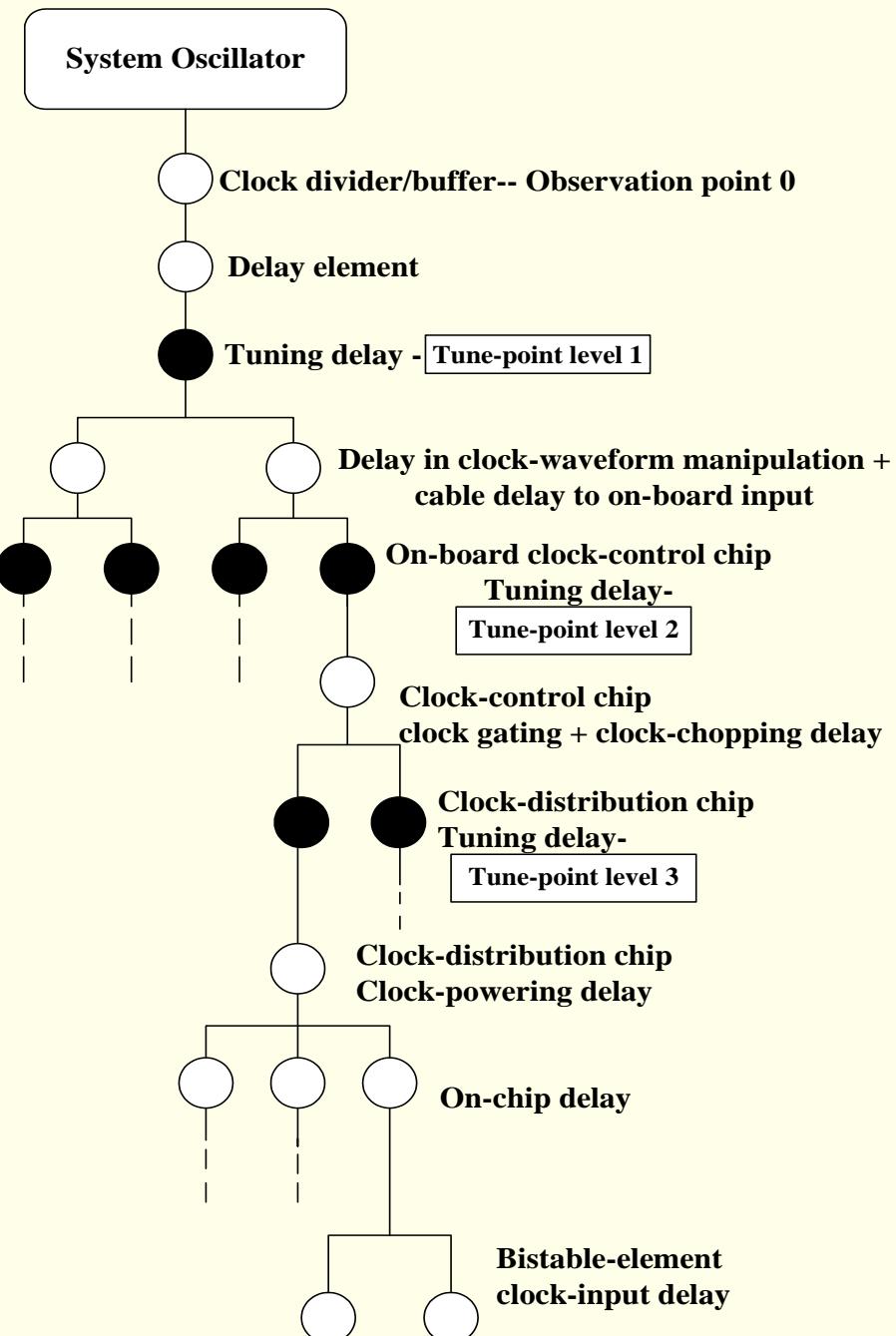


The Concept of Logic Islands (Wagner 1988), Copyright © 1988 IEEE



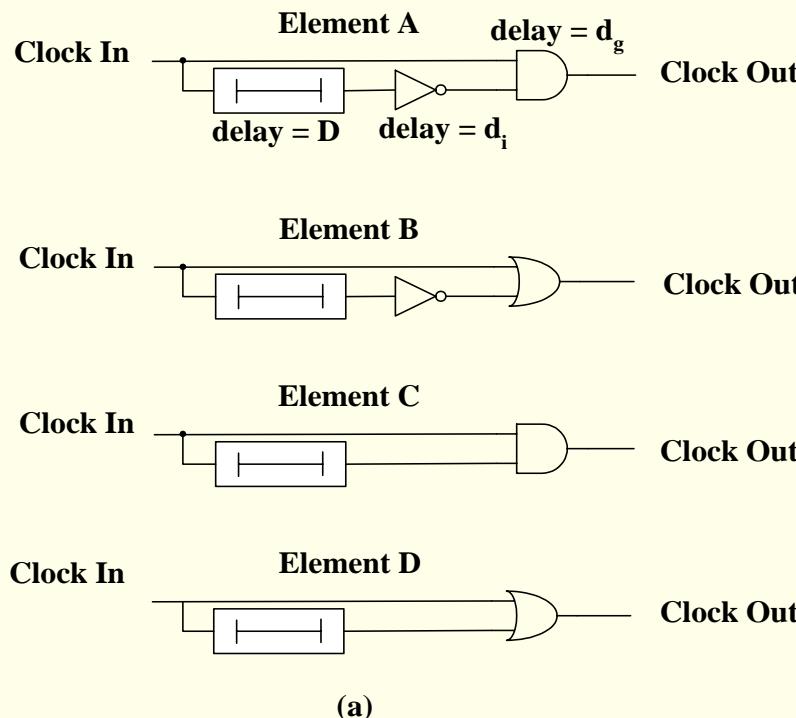
Clock Tuning Points

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IEEE

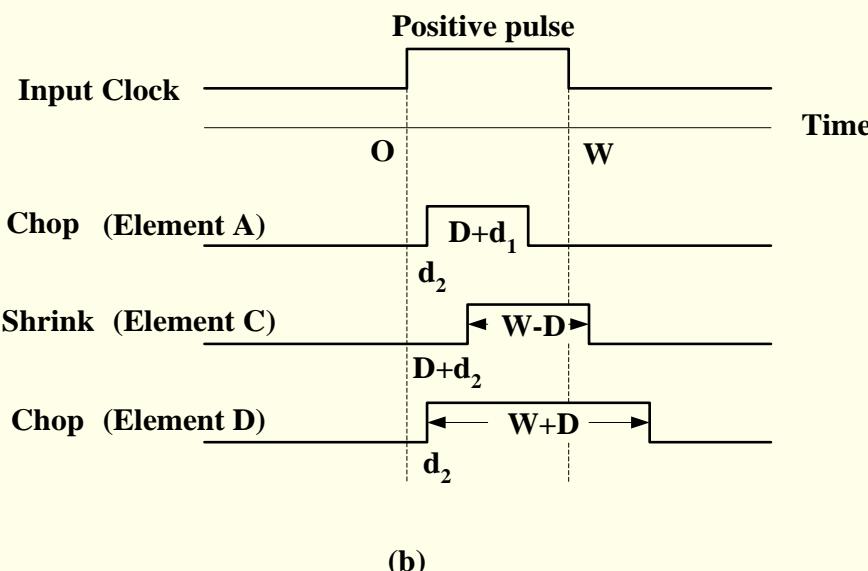


Various Clock Shaping Elements and Obtained Clock Signals.

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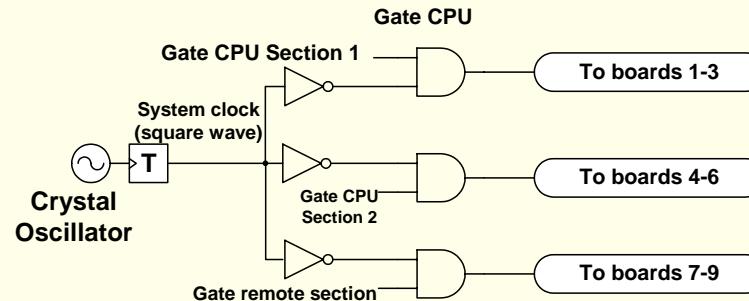


(a)

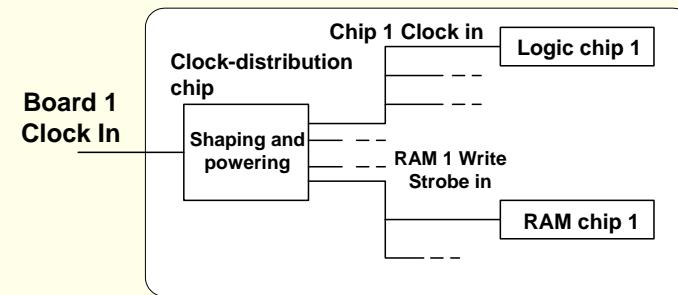


(b)

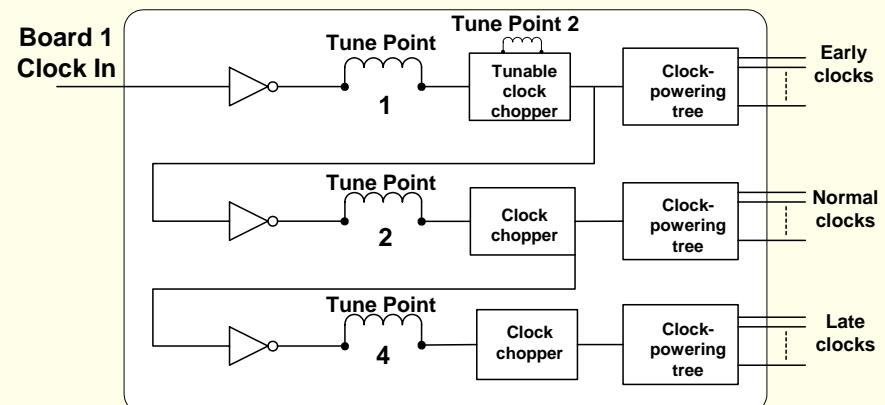
*Clock distribution network
within a system,
(b) on the board, and
(c) tuning of the clock.
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(a)



(b)

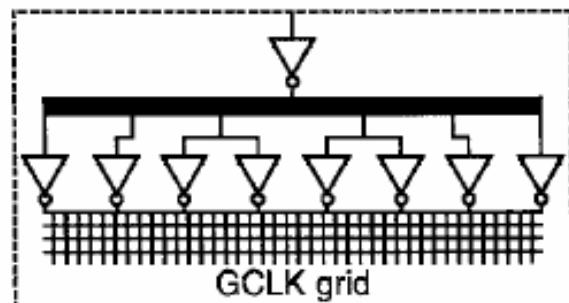
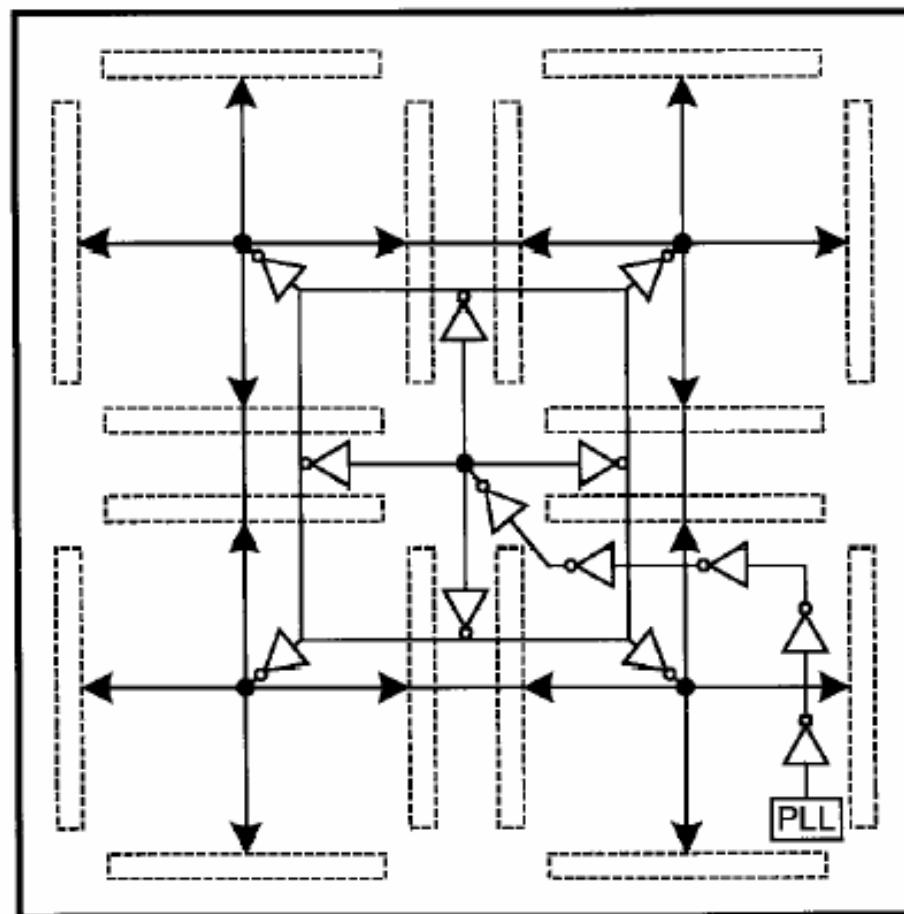


(c)

Clock distribution methods:

(a) an RC matched tree, and (b) a grid

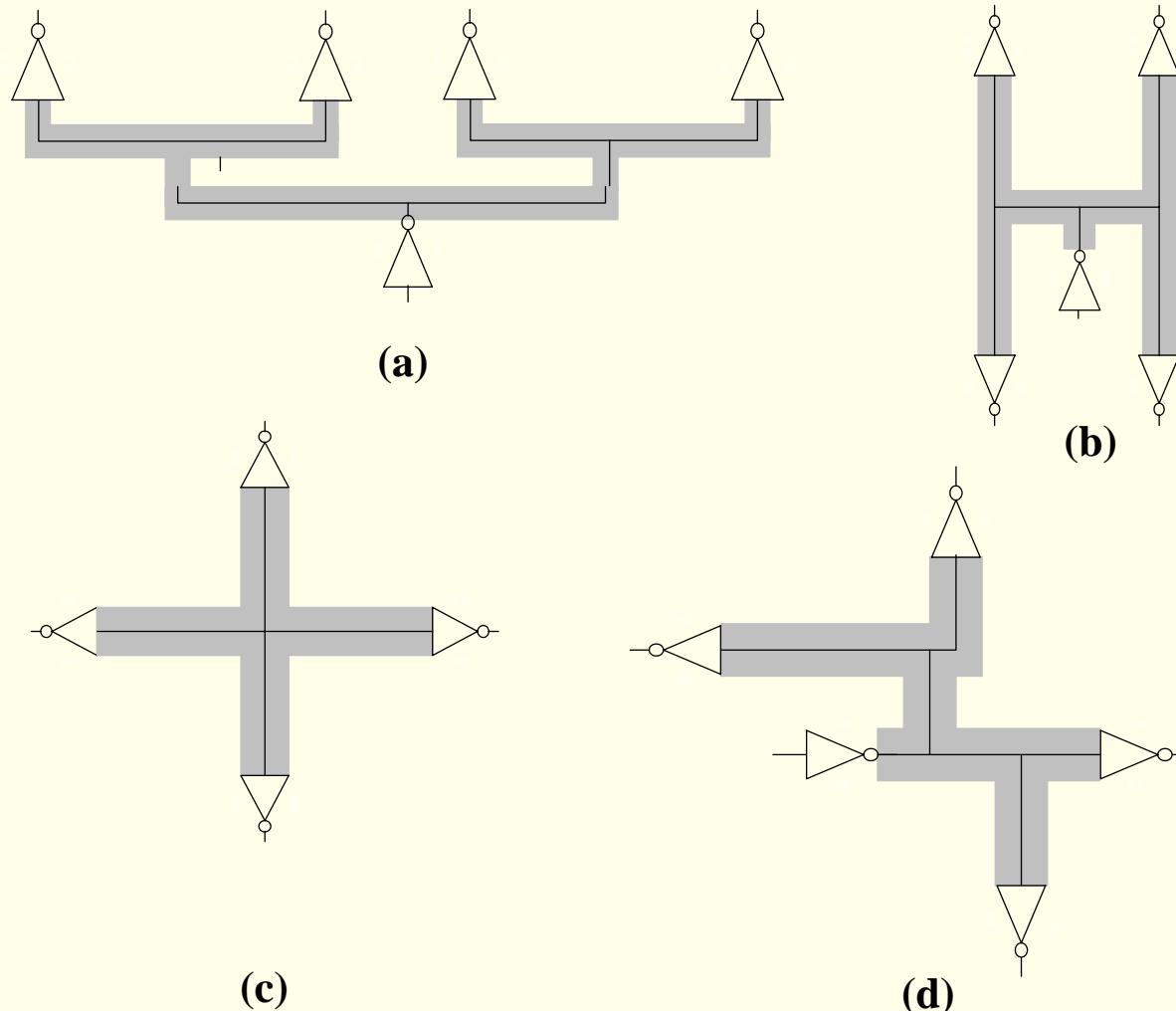
(Bailey and Benschneider 1998), Copyright © 1988, IEEE



RC delay matched clock distribution topologies:

(a) a binary tree, (b) an H tree, (c) an X tree, (d) an arbitrary matched RC matched tree

(From Bailey in Chandrakasan et al. 2001), Copyright © 1988, IEEE



Clock distribution grid used in a DEC Alpha 600-MHz processor

(Bailey and Benschneider 1998), Copyright © 1988, IEEE

