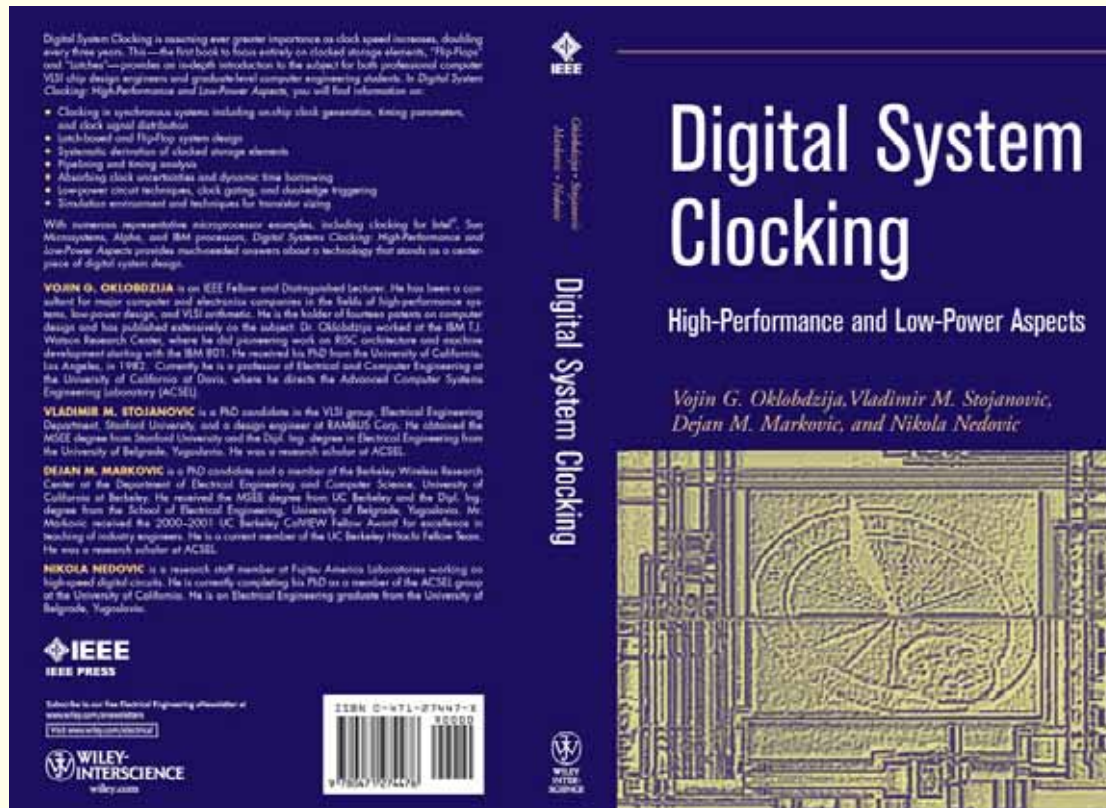


Digital System Clocking:

High-Performance and Low-Power Aspects

Vojin G. Oklobdzija, Vladimir M. Stojanovic, Dejan M. Markovic, Nikola M. Nedovic

Chapter 6: Low-Energy System Issues



Wiley-Interscience and IEEE Press, January 2003

Switching Energy

Clock is the highest activity signal \Rightarrow Switching energy is dominant

$$E_{\text{switching}} = \sum_{i=1}^N \alpha_{0-1}(i) \cdot C_i \cdot V_{\text{swing}}(i) \cdot V_{DD}$$

α - probability of a 0-1 transition

C_i - total switched capacitance at node i

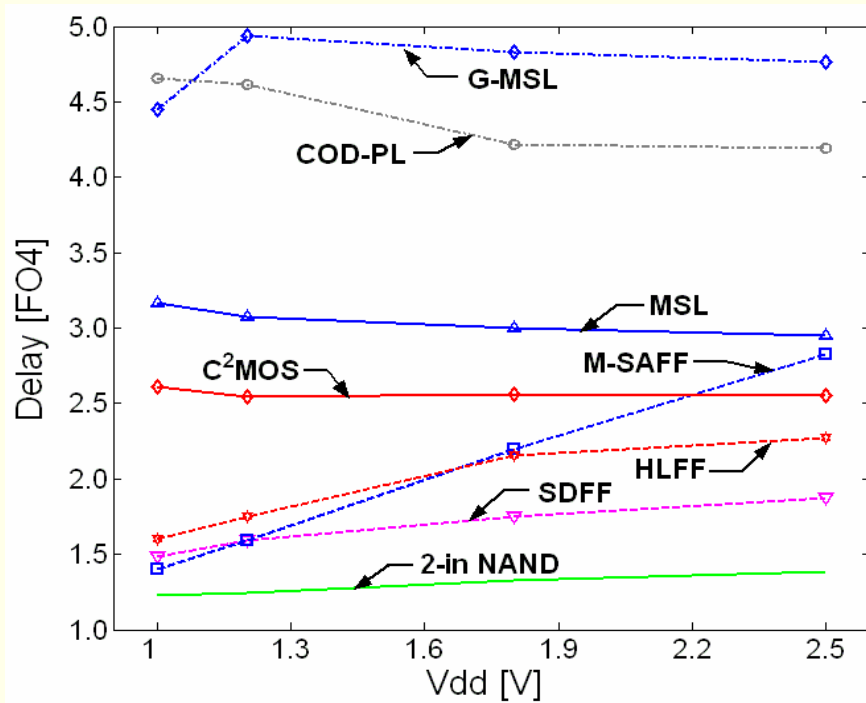
$V_{\text{swing}}(i)$ - voltage swing at node i

V_{DD} - supply voltage

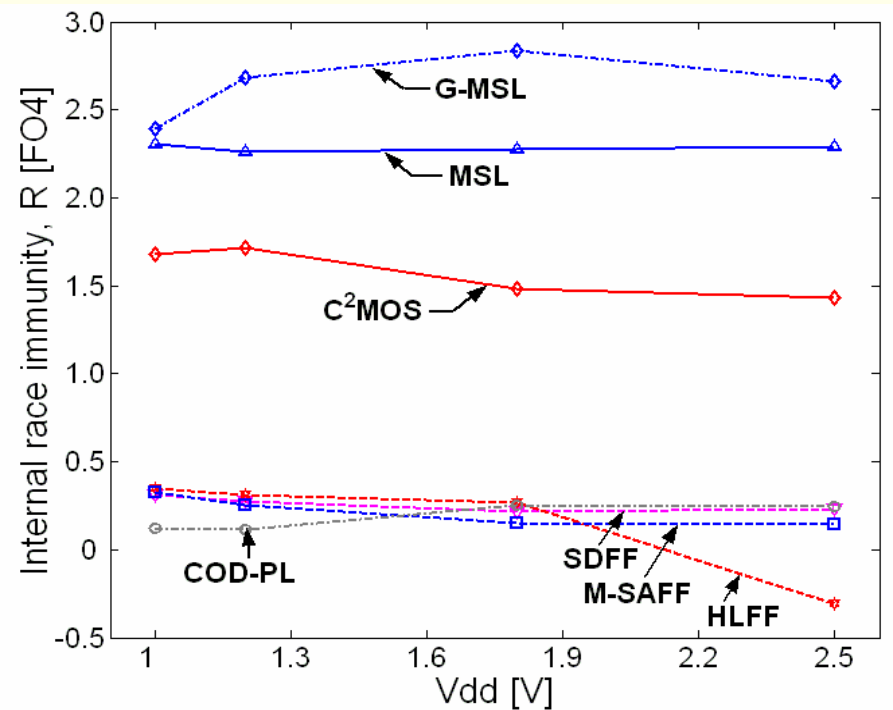
N - number of nodes

*Energy is best reduced by scaling down V_{DD} ,
but this also means performance degradation*

Pulsed Designs Scale the Best with V_{DD}



(a)



(b)

(Delay is normalized to FO4 at its respective V_{DD} . FO4 as defined in this example increases with $V_{DD} \Rightarrow$ performance degradation)

Impact of V_{dd} on (a) delay, and (b) internal race immunity (0.25 μm , light load). (Markovic et al. 2001), Copyright © 2001 IEEE

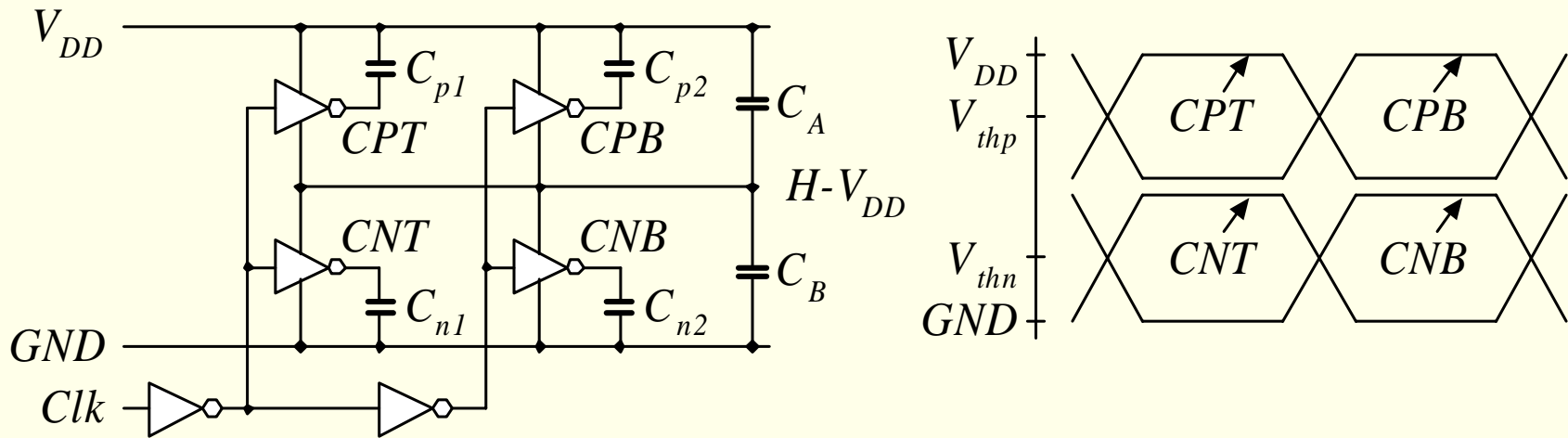
Other Energy Reduction Techniques

- Low-Swing Circuit Techniques
 - Reduced-swing Clk drivers
 - CSE redesign
 - N-only CSEs with Low-Vcc Clk
- Clock Gating
 - Global
 - Local
- Dual-Edge Triggering
 - Latch-mux
 - Pulsed-latch
 - Flip-flop

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Low-Swing Clocking, Option #1: Clock Driver Re-design

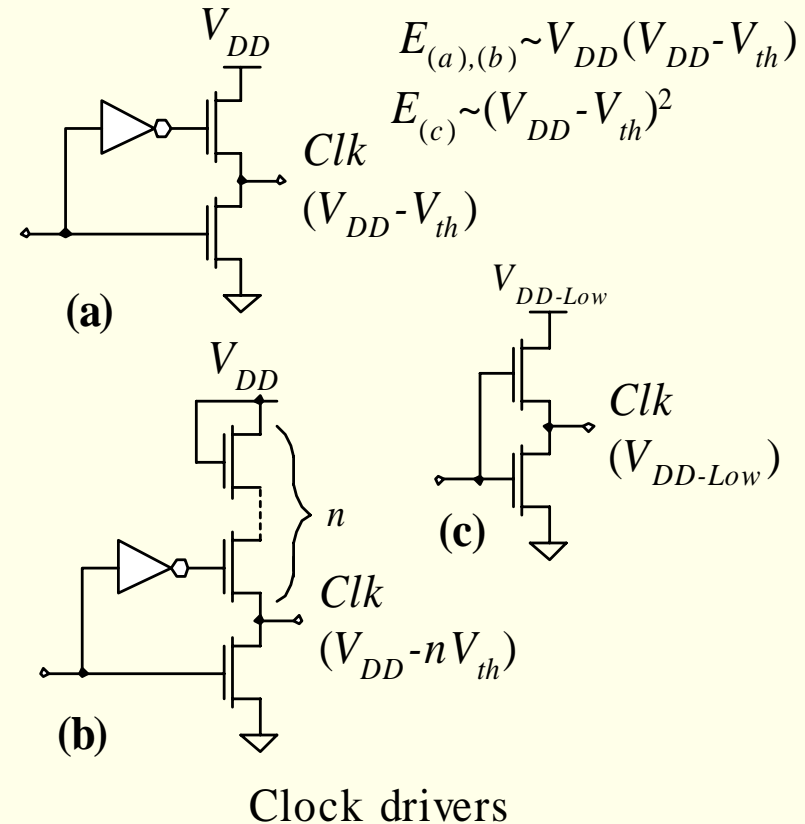
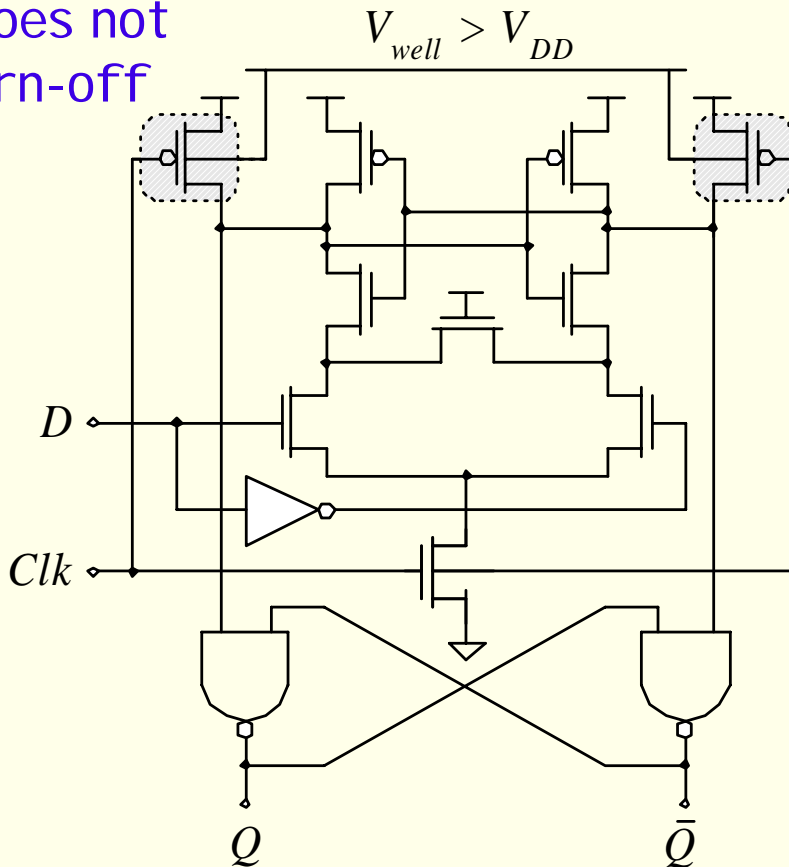


50% power reduction with half-swing clock
(minus some penalty in clock drivers)

*Clock driver for half-swing clocking
(Kojima et al. 1995), Copyright © 1995 IEEE*

Low-Swing Clocking, Option #2: CSE Re-design

PMOS does not
fully turn-off

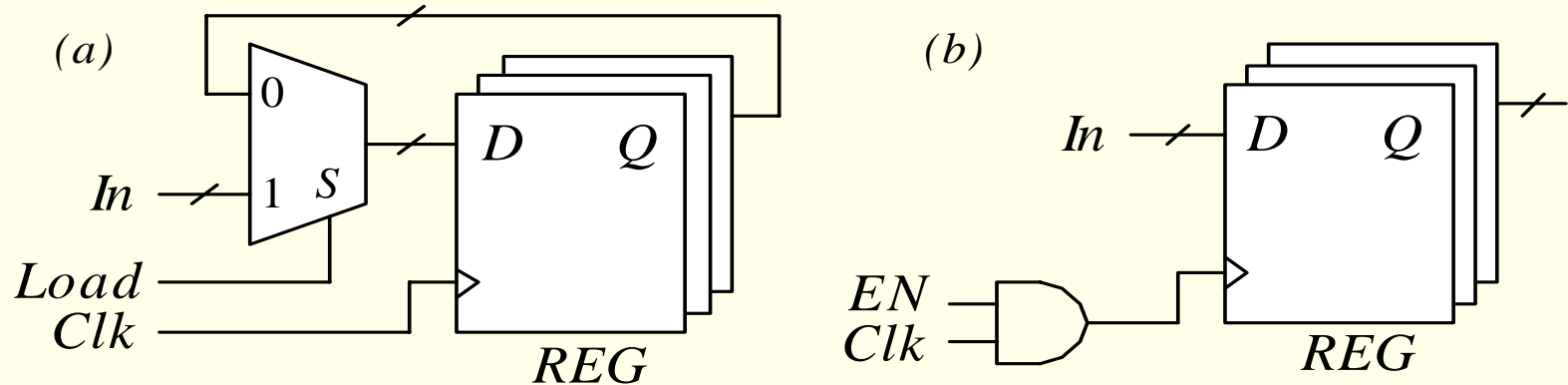


Reduced clock-swing flip-flop
(Kawaguchi and Sakurai, 1998), Copyright © 1998 IEEE

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Clock Gating, Option #1: Global Clock Gating



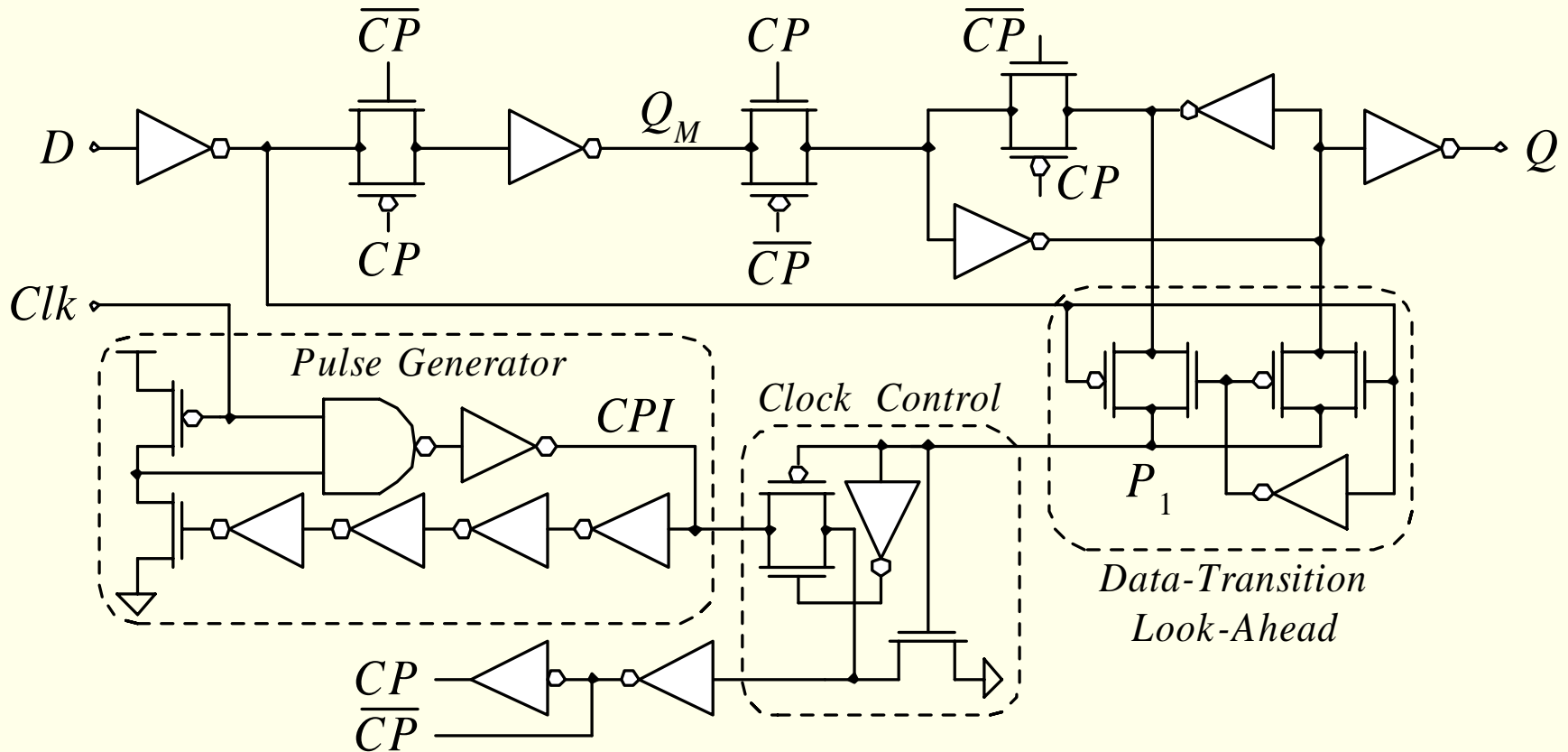
Time-mux
(no gating!)

Global Clk Gating

Used to save clocking energy when data activity is low

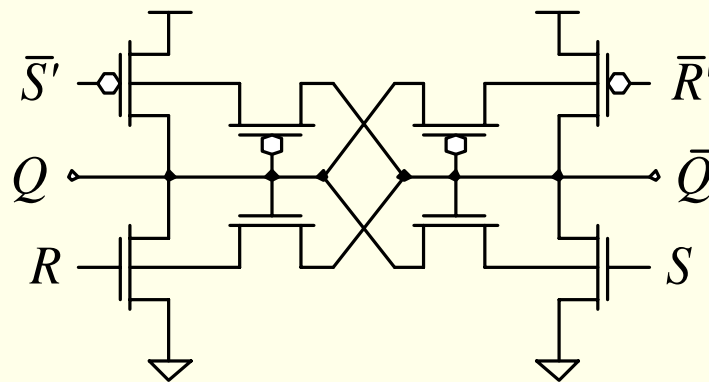
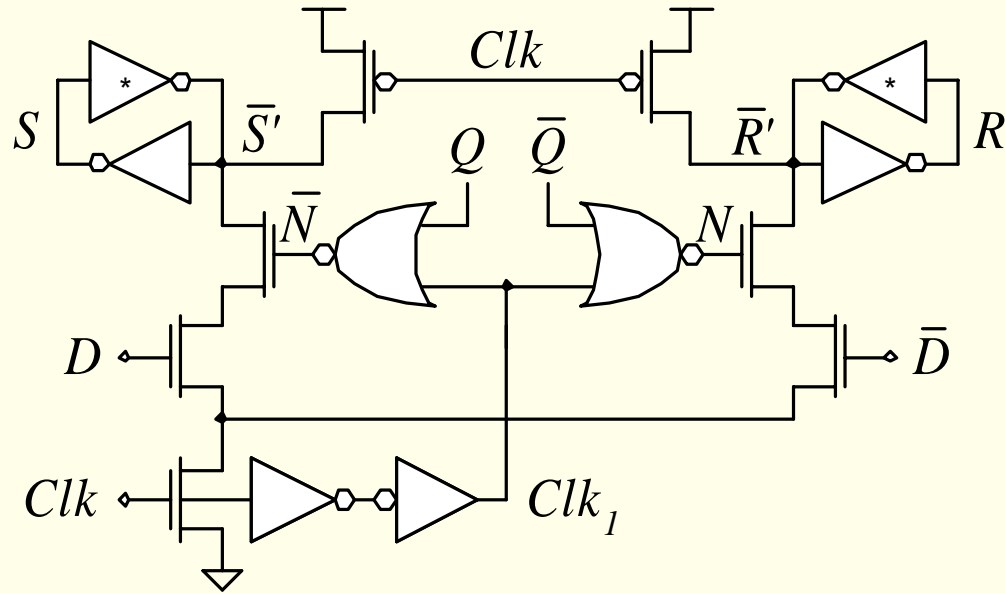
*(a) Nongated clock circuit, (b) gated clock circuit.
(Kitahara et al. 1998), Copyright © 1998 IEEE*

Clock Gating, Option #2: Local Clock Gating



*Data-transition look-ahead latch
(Nogawa and Ohtomo, 1998), Copyright © 1998 IEEE*

Local Clock Gating, Another Example

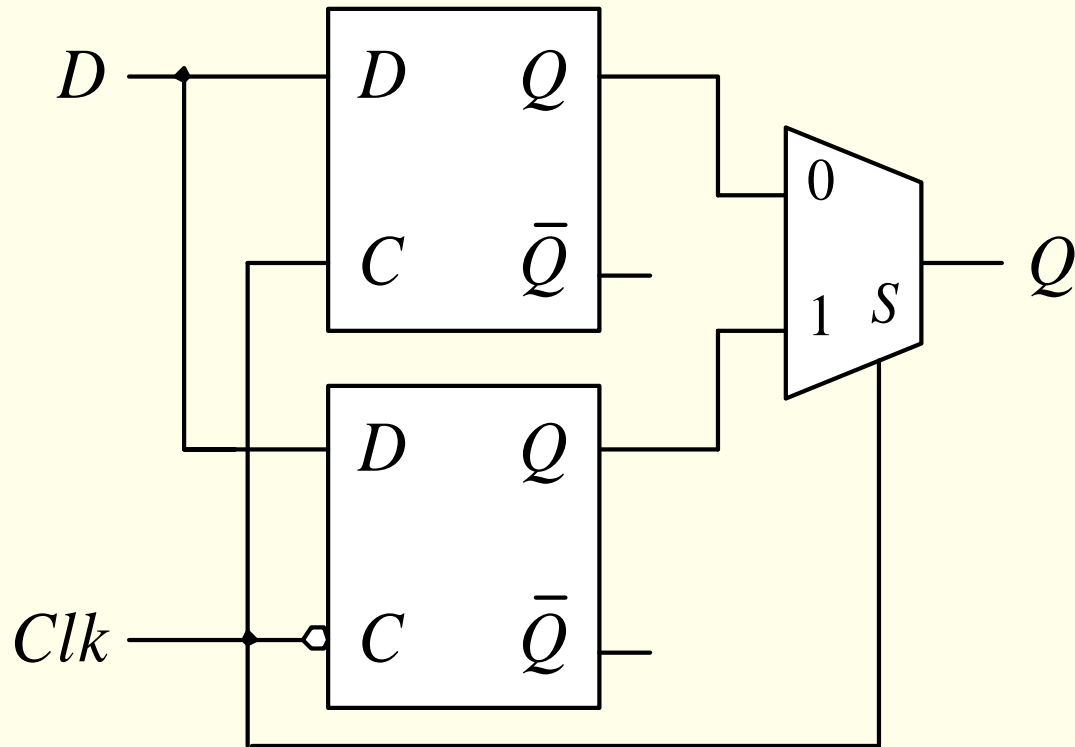


*Conditional capture flip-flop
(Kong et al. 2000), Copyright © 2000 IEEE*

Other Energy Reduction Techniques

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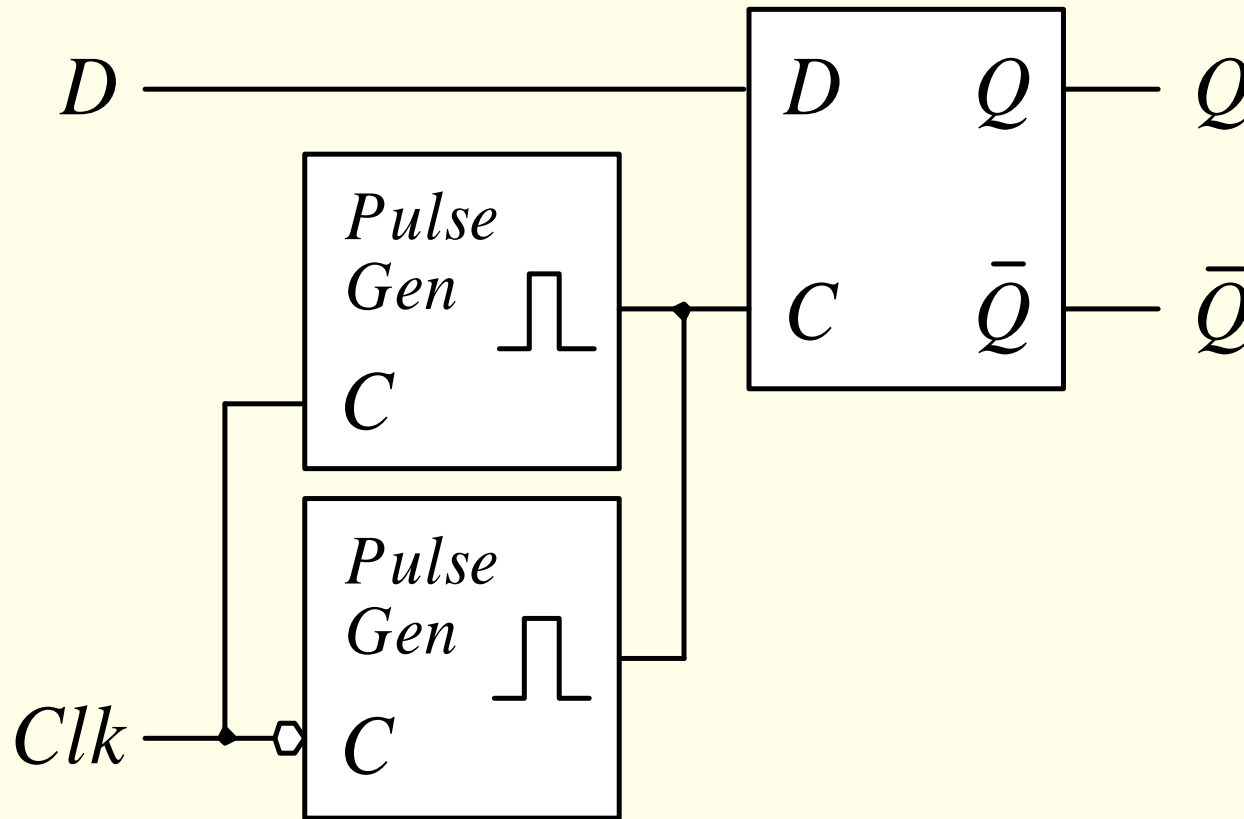
Dual-Edge Triggering, Option #1: Latch-Mux



Used to save clocking energy regardless of data activity!

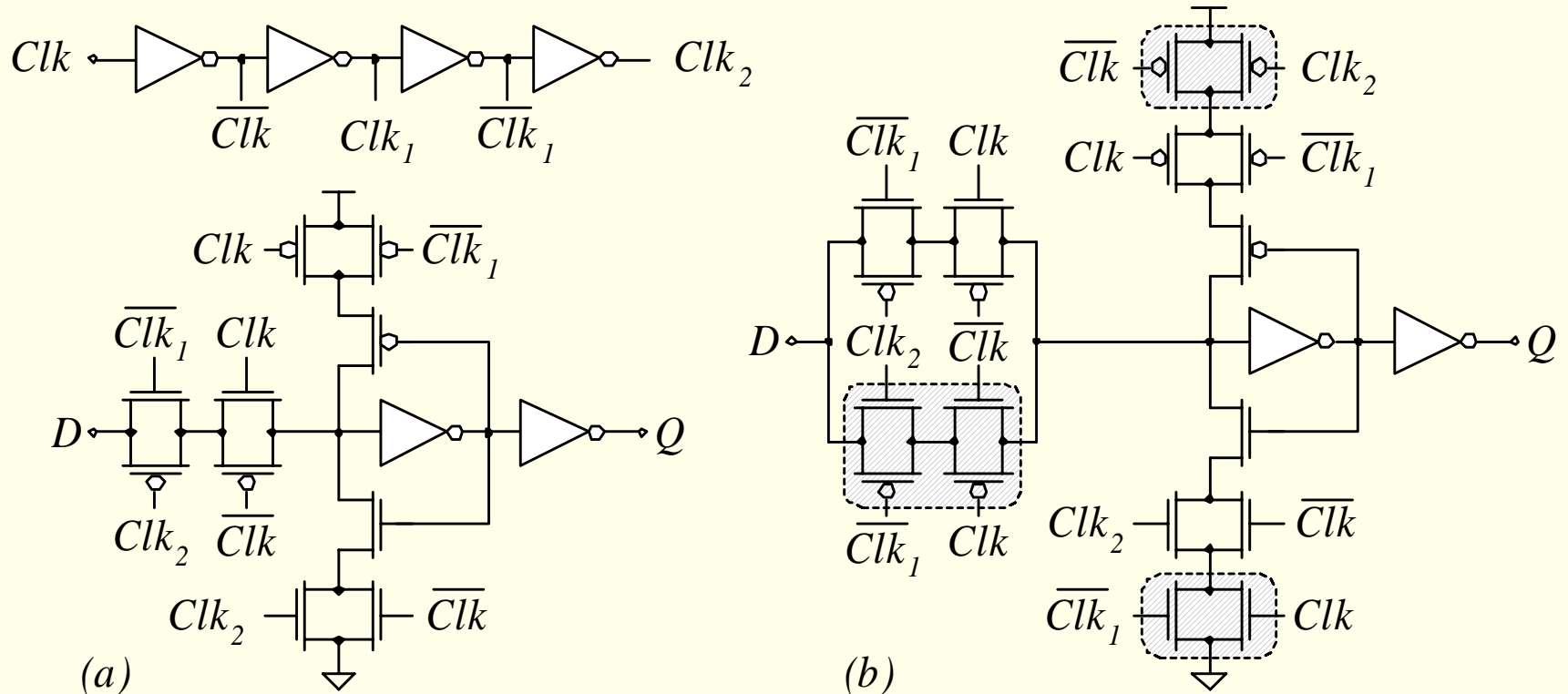
Dual-edge-triggered latch-mux design

Dual-Edge Triggering, Option #2: Pulsed-Latch



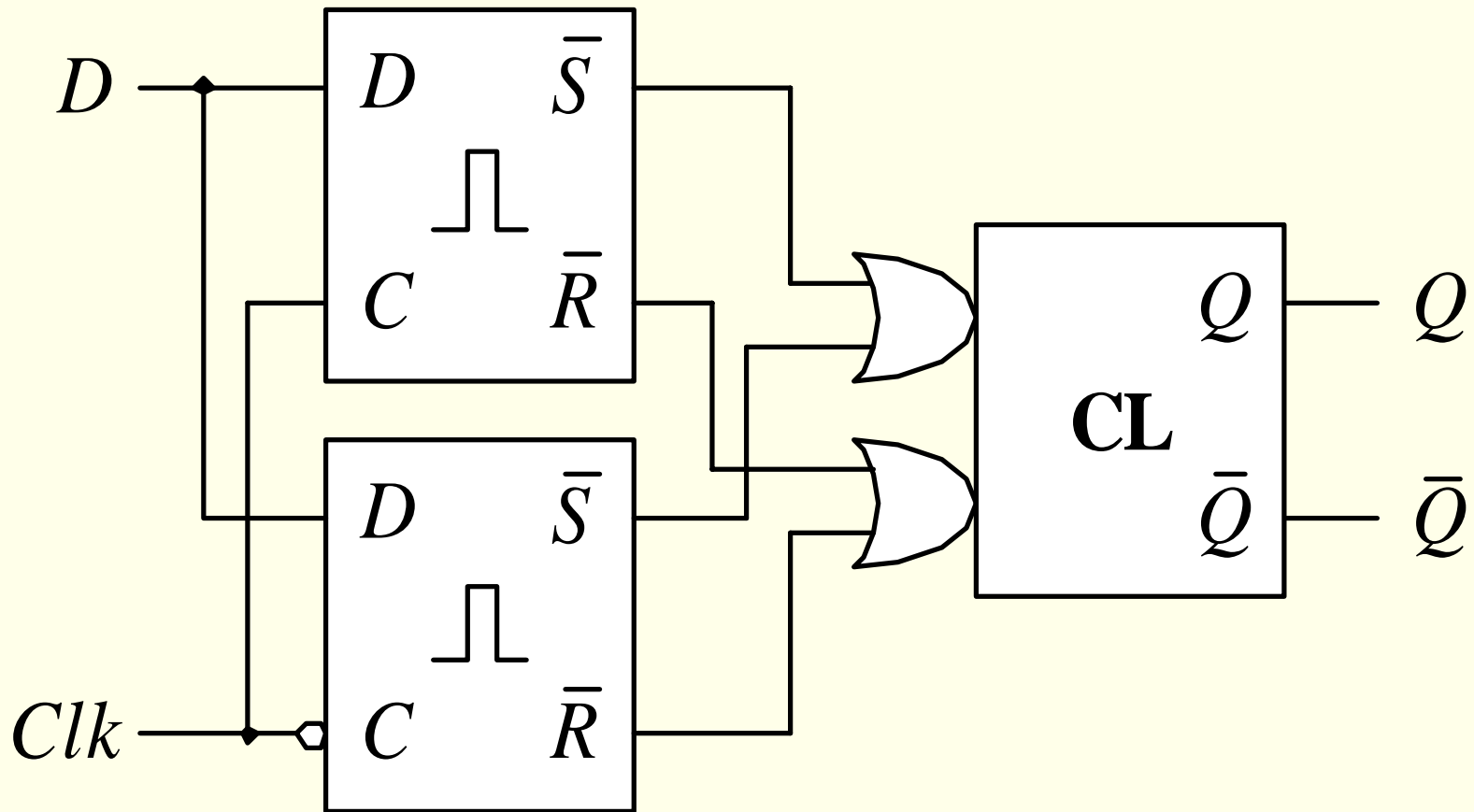
Dual-edge-triggered pulsed-latch design

DET Pulsed-Latch: Circuit Examples



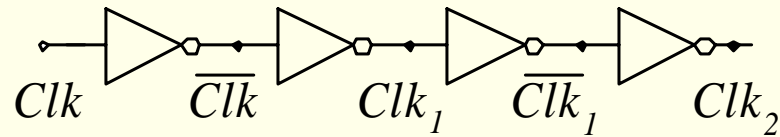
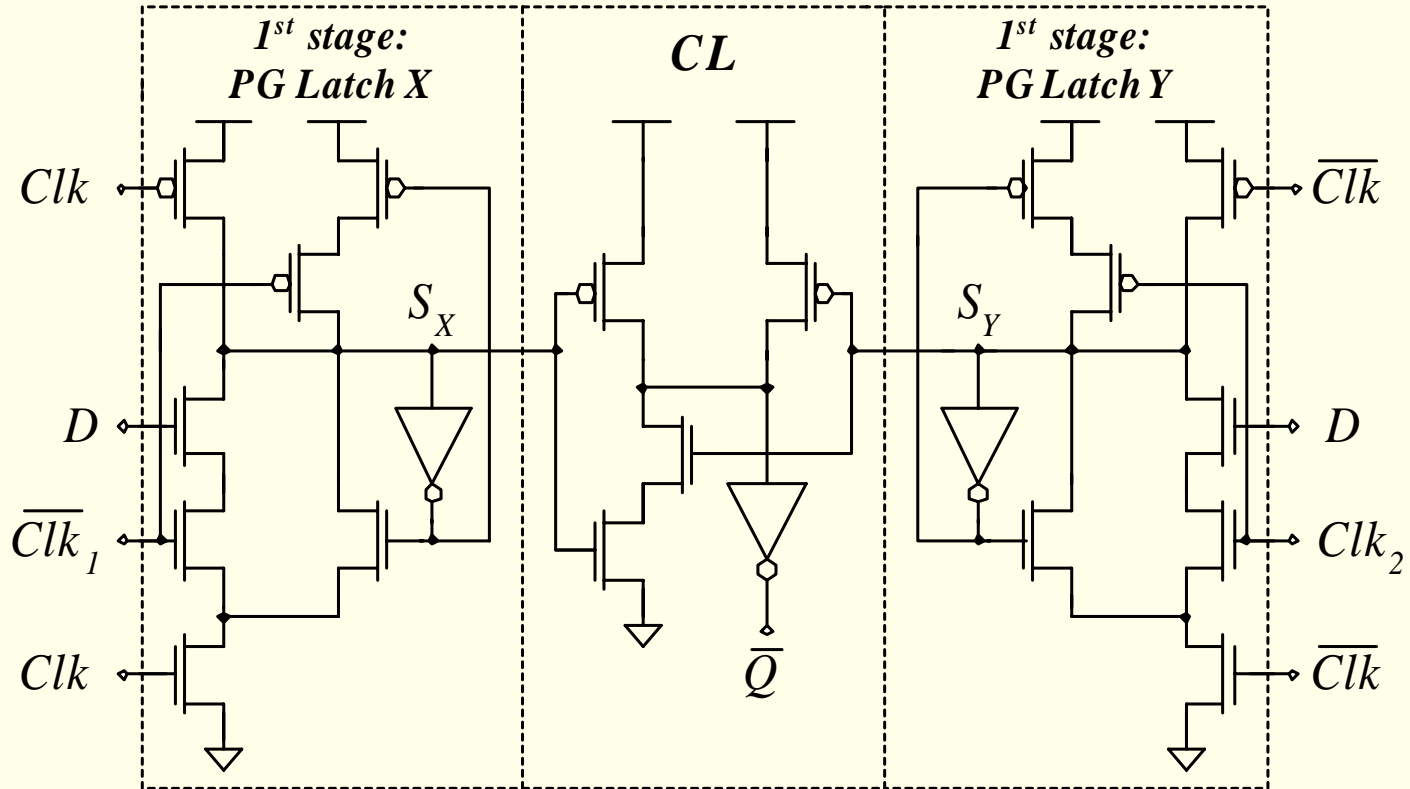
Pulsed-latch: (a) single-edge-triggered; (b) dual-edge-triggered

Dual-Edge Triggered Flip-Flop



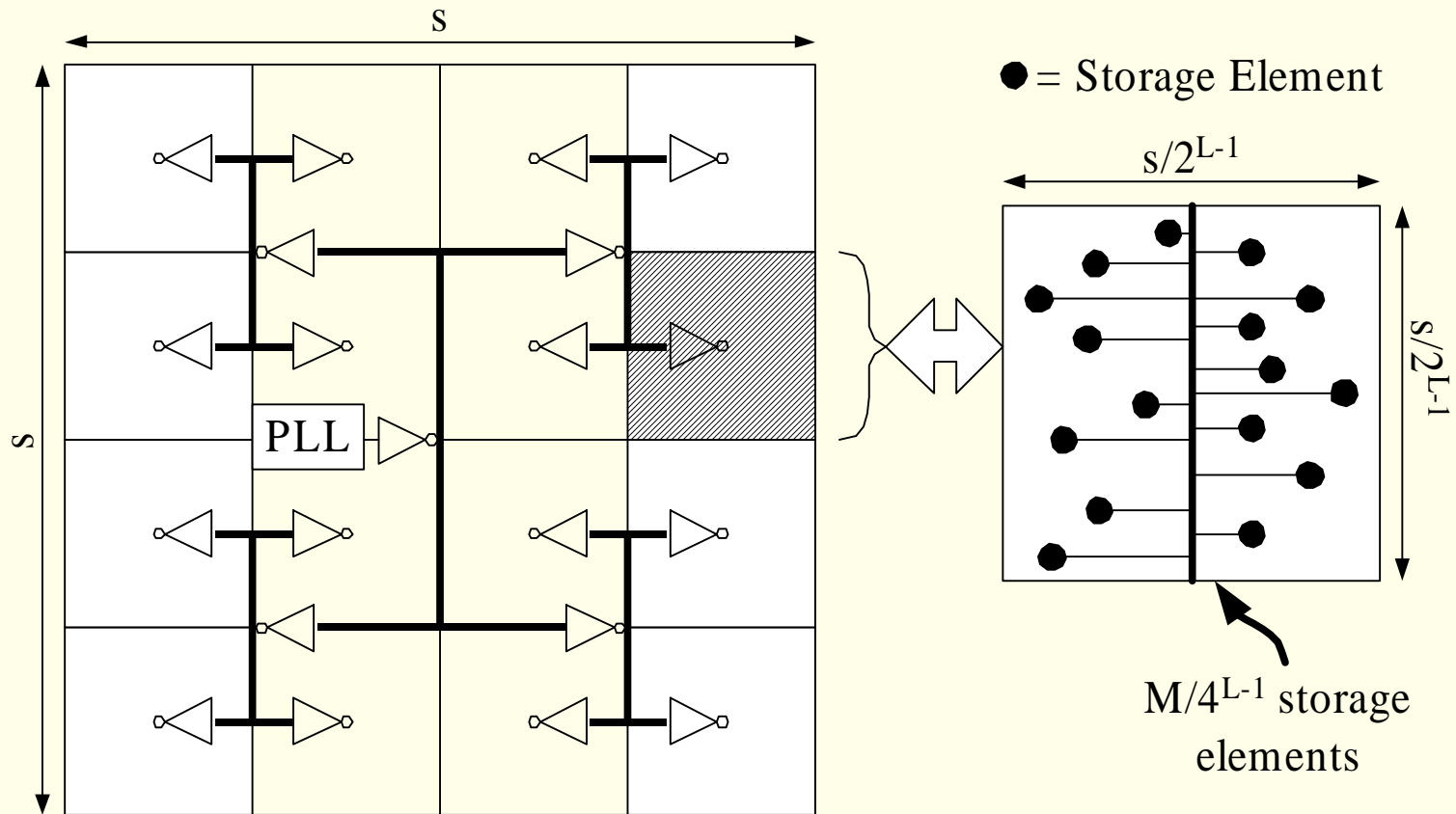
Dual-edge-triggered flip-flop design

DET Flip-Flop: Circuit Example



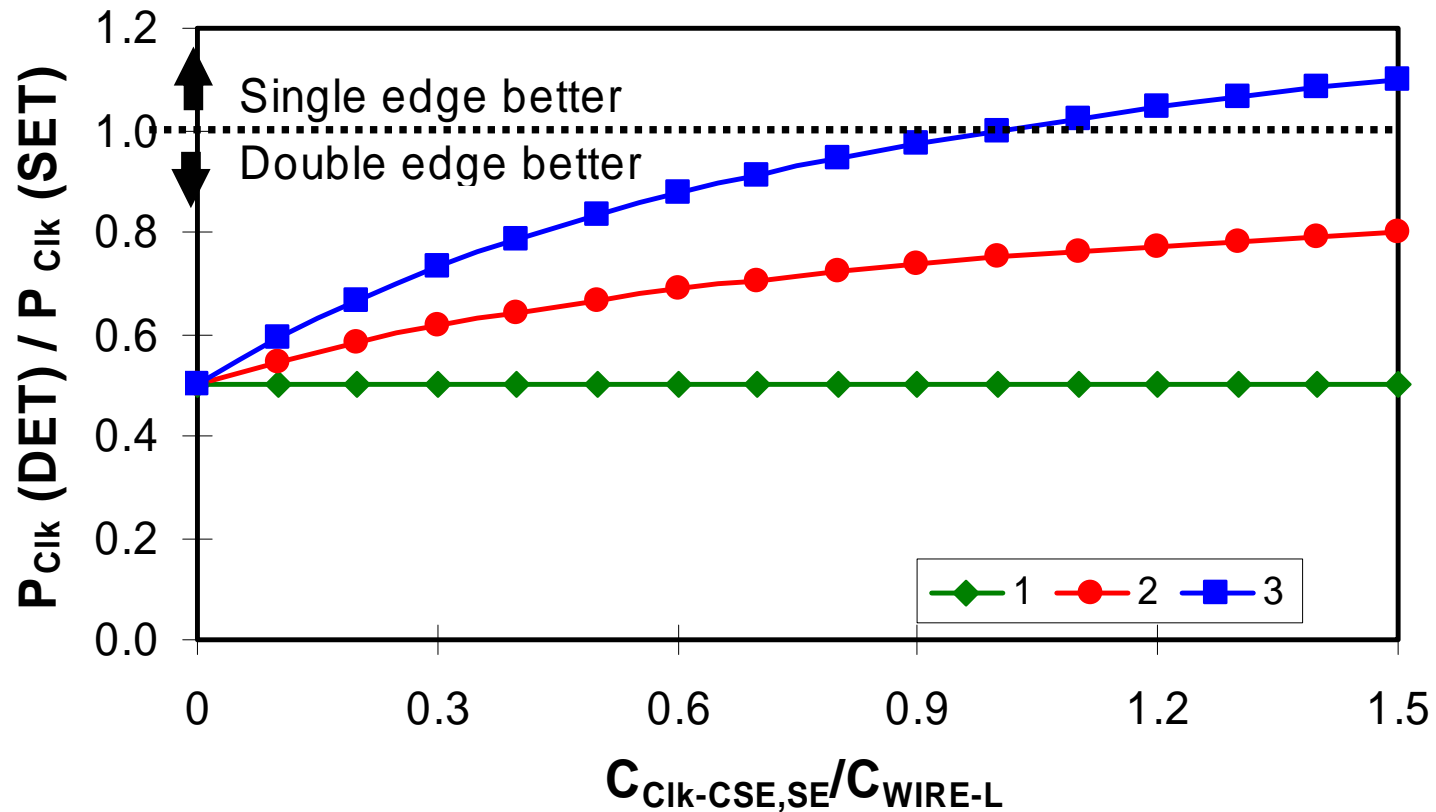
DET symmetric pulse-generator flip-flop

Clock Distribution



H-tree clock distribution network

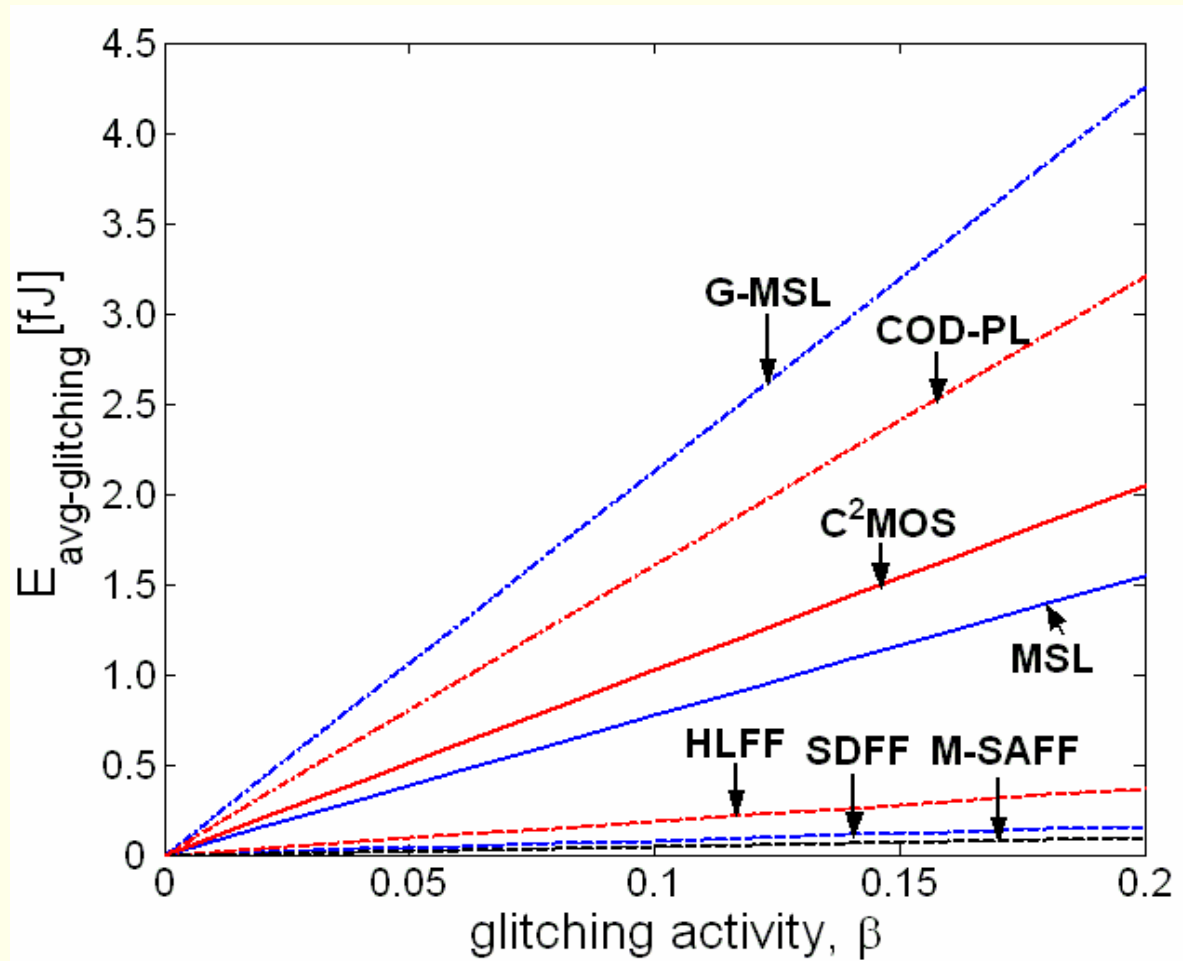
Clocking Power: SET vs. DET



Clocking power in single- and dual-edge-triggered systems

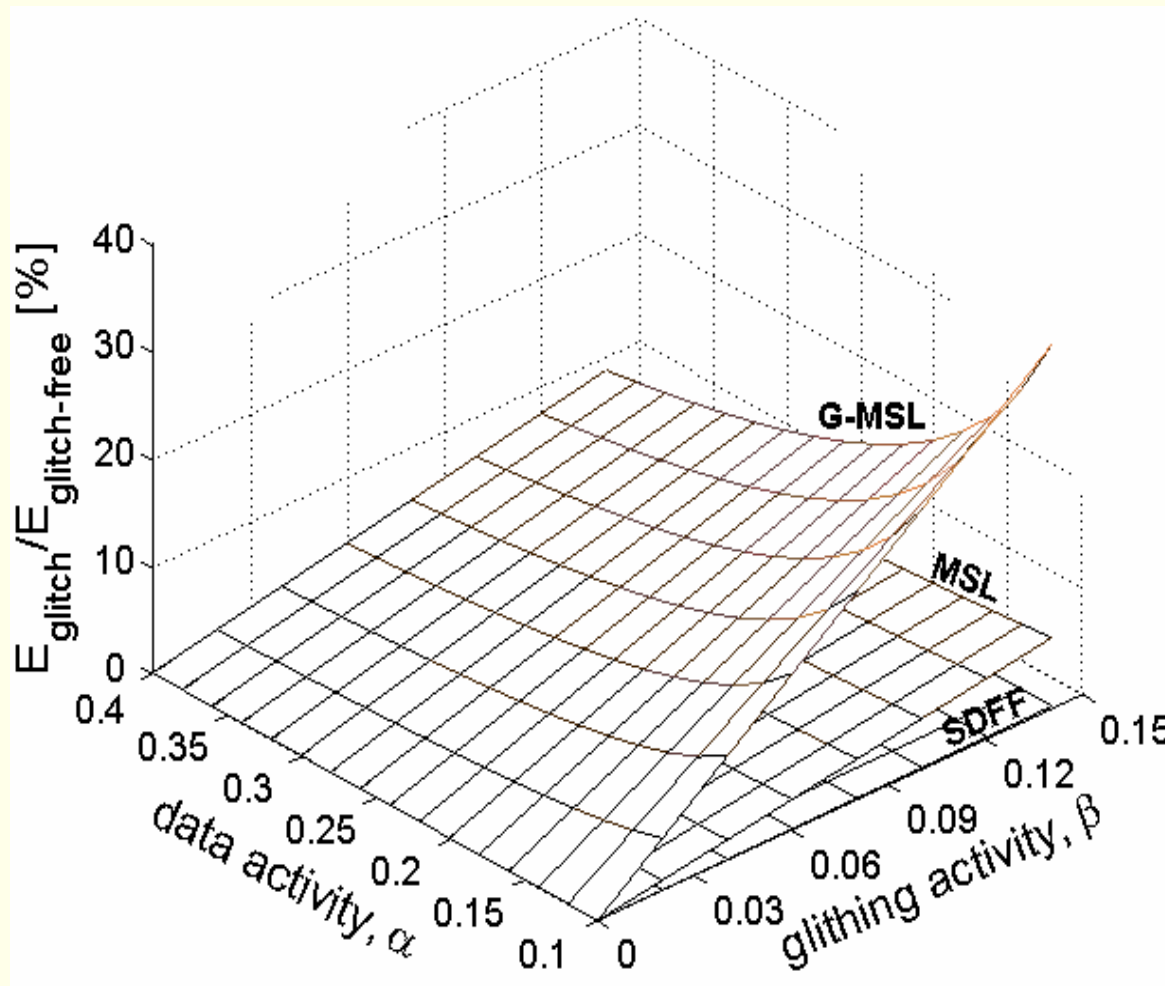
Glitch Robust Design

Average Glitching Energy in CSEs



*Comparison of average glitching energy in CSEs
(Markovic et al. 2001), Copyright © 2001 IEEE*

Comparison of $E_{\text{glitching}}$ and $E_{\text{switching}}$



Glitching energy as a percentage of switching energy in representative CSEs showing the greatest glitch sensitivity of the gated designs

Summary

- Energy best reduced by V_{DD} scaling
 - Penalty in performance
- Reducing Clk swing only reduces E_{CLK}
 - Still penalty in performance
- Clock gating
 - Reduces E_{CLK} at low-activity
 - No penalty in perf. if gating is outside crit-path
- Dual-Edge Triggering
 - Reduces E_{CLK} ideally by 2x
 - Small or no performance degradation