I. ENERGY OPTIMIZATION FOR LINEAR SYSTEMS

For simplicity, the energy optimization is first developed for the linear multi-path circuit. It is assumed that loading to any node of the system is purely gate input, except at the output. The output load is fixed whereas the input is allowed to vary.

1. DEFINITION

An n-stage system is linear when the output load is proportional to the size of all gates in the system and the stage efforts of the later output stages. That is,

$$W_{Load} \propto W_{gate,i} * \prod_{j=i}^{n} f_j , \quad \text{for } i = 1 \rightarrow n$$

2. THEOREM

A system is linear if and only if loads to any gates are inversely proportional to the stage efforts of the later output stages.

Proof:

By definition, if the system is linear, the theorem is true. We only need to prove the reverse. It is done by induction method on the stages as followed.

* At i=n:

$W_n = W_{Load} / f_n \Leftrightarrow W_{Load} = W_n f_n$

So, the final stage satisfies the linear condition.

* Assume the linear condition is satisfied for all stages i ≥ k+1. That is,

$$W_{Load} \propto W_{gate,k+1} \prod_{j=k+1}^{n} f_j$$

* For an arbitrary gate in stage k, which is loaded by m gates in stage (k+1),

$$W_{gate,k} = \frac{1}{f_k} \sum_{j=1}^{m} \beta_j W_{k+1,j} , \; with \; \beta_j = const.$$

$$\propto \frac{1}{f_k} \sum_{j=1}^{m} \beta_j \frac{W_{Load}}{\prod_{j=k+1}^{n} f_j} \propto \frac{W_{Load}}{\prod_{j=k}^{n} f_j}$$

Therefore, by induction, the theorem is proved.

3. COLLOQUIUM

In a linear system, the load is proportional to the total size of any stage and the stage efforts of the later output stages. That is,

$$W_{Load} \; \alpha \; \Sigma W_{stage\,i} * \prod_{j=i}^{n} f_j , \text{ for } i = 1 \rightarrow n$$

It can be shown that when sizing of a system is solely based on its own gate size, the system is linear. When wiring capacitance is included, the system becomes non-linear.

4. ENERGY OPTIMIZATION FOR MULTI-PATH LINEAR SYSTEM

Assume a linear system consisting of m-input n-stage multi-path circuit, Figure 1. A fixed load C_{out} is represented by an equivalent gate size W_{out}.

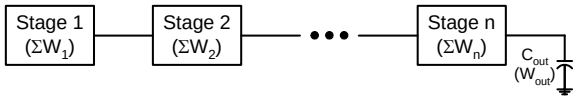

Figure 1: Circuit structure of a multi-path system

One solution for a target delay can be obtained by using equal stage effort for all stages in the system.

Since the system is linear, the size of an arbitrary gate j at stage i is

$$W_{i,j} = \frac{k_{i,j} W_{out}}{f^{n+1-i}} \quad (1)$$

where $k_{i,j}$ is constant, depending only gate characteristics in the system.

The input stage corresponds to i=1. Its size is determined by

$$W_{dr} = W_1 = \frac{k_1 W_{C,n}}{f^n}$$

The total delay is

$$T_{d,Total} = \sum_{i=1}^{n} (f + p_i) \quad (2)$$

The total energy is found using equation (d):

$$E_{Total} = \sum_{i=1}^{n} \sum_{j} c_{g(i,j)} W_{g(i,j)} + E_{wire} = \sum_{i=1}^{n} E_i + E_{wire}$$
$$where \quad E_i = \sum_{j} c_{g(i,j)} W_{g(i,j)} \quad (3)$$

The E_i term is the energy associated with gate sizes in stage i.

To achieve lower energy consumption at the same performance, the effort of each stage is varied by a factor y_i. That is,

$$f_i = y_i f, \text{ with } y_i \in (0, n), \text{ for } i = 1 \rightarrow n \quad (4)$$

The lower bound of y_i is due to the positive value of stage effort *f*. Its upper bound is proved later.

The new gate sizes, input size and the total delay are

$$W_{i,j}(y) = \frac{W_{i,j}}{\prod_{j=i}^{n} y_j} \quad (5)$$

$$W_{dr}\{y\} = \frac{W_0}{\prod_{j=1}^{n} y_j} \quad (6)$$

$$T_{d,Total}\{y\} = \sum_{i=1}^{n} (y_i f + p_i) \quad (7)$$

To maintain the same performance, it is necessary that (2) and (7) are equal. Then,

$$T_{d,Total}\{y\} = T_{d,Total} \Leftrightarrow \sum_{i=1}^{n} y_i - n = 0 \quad (8)$$

(8) is called the equal-delay constraint C. As the lower bound of each y_i is 0 and due to constraint (8), the upper bound of y_i is n – as shown below.

$$(8) \Rightarrow y_j = -\sum_{i \neq j, i=1}^{n} y_i + n < n$$

The new total energy becomes

$$E_{Total}\{y\} = \sum_{i=1}^{n} \sum_{j} c_{g(i,j)} \frac{W_{g(i,j)}}{\prod_{p=i}^{n} y_i} + E_{wire}$$

$$E_{Total}\{y\} = \sum_{i=1}^{n} \frac{E_j}{\prod_{p=i}^{n} y_i} + E_{wire} \quad (10)$$

The minimal energy solution is found by minimizing (9) under constraint (8). It is solved using LaGrange method.

$$F = E_{Total}\{y\} + \lambda C \quad (11)$$

where λ is the LaGrange multiplier. The solution is found by solving (8) and n partial derivative equations:

$\partial F/\partial x_i = 0$ (for $i = 1 \rightarrow n$) (**12**)

These derivatives can be algebraically simplified to

$$E_1 = \lambda y_1 \prod_{j=1}^{n} y_j \quad \textbf{(11.1)}$$

$$E_1 + E_2 y_1 = \lambda y_2 \prod_{j=1}^{n} y_j \quad \textbf{(11.2)}$$

(…)

$$E_1 + \sum_{i=2}^{n-1} \left(E_i \prod_{j=1}^{i-1} y_j \right) = \lambda y_n \prod_{j=1}^{n} y_j \quad \textbf{(11.n)}$$

Equations (11.1)–(11.n) can be simplified further by combining adjacent pairs. The results are

$$E_1 (y_2 - y_1) = E_2 y_1^{\,2} \quad \textbf{(13.1)}$$

$$(E_1 + E_2 y_1)(y_3 - y_2) = E_3 y_1 y_2^{\,2} \quad \textbf{(12.2)}$$

(…)

$$\left[E_1 + \sum_{i=2}^{n-1} \left(E_i \prod_{j=1}^{i-1} y_j \right) \right] (y_n - y_{n-1}) = E_n y_{n-1} \prod_{j=1}^{n-1} y_j \quad \textbf{(12.n-1)}$$

Note that equations (12.1) through (12.n-1) are a lot simpler, where factor y_i is determined solely from preceded $y_j < y_i$ and initial sizing. Minimal energy solution is obtained by numerically solving equations (8), (11.1) and (12.1) through (12.n-1).

5. ESTIMATE OF RUN TIME

The proposed method is significantly faster compared to the traditional optimization tools because it has eliminated the iterative and costly process of gate resizing. Each gate size is computed only twice: (i) to obtain the initial value and (ii) to find the optimal solution. That results in constant run time on gate sizing.

The iteration is moved to the optimization process and is done only once. In addition, the number of variables is reduced to the number of stages. With the computing power nowadays, this process takes no time at all.

Overall, in term of big-O notation, the run time of the optimization is O(n) where n is the number of stages.

II. ENERGY OPTIMIZATION FOR NON-LINEAR SYSTEM

Real circuits are often not linear. Long wire connection between nodes introduces constant loading that is not scaled with the output load. Therefore, the method is next modified to accommodate this scenario.

Assume a datapath consisting of m-input n-stage multi-path circuit, Figure 2. The fixed output load C_{Load} is represented by an equivalent gate size $W_{C,n}$ and the global wire capacitance between stages i and (i+1) by $W_{C,i}$.

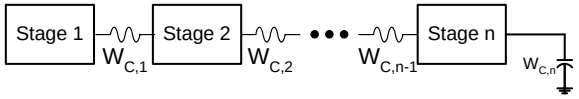

Figure 2: n-stage datapath including wire capacitance

One solution for a desirable delay can be obtained by using equal stage effort for all stages.

Straightforwardly, the size of gate k in final stage n is given by

$$W_{n,k} = \frac{g_{n,k} W_{C,n}}{f} \tag{14}$$

Similarly, the size of an arbitrary gate k in stage (n-1) is computed with the load from gates in stage n and the load by the global wire capacitance $W_{C,n-1}$.

$$W_{n-1,k} = \frac{g_{n-1,k}\left(\sum_p \chi_p W_{n,p} + W_{C,n-1}\right)}{f} \tag{14.1}$$

$$= g_{n-1,k}\left(\sum_p \chi_p g_{n,p}\right)\frac{W_{C,n}}{f^2} + g_{n-1,k}\frac{W_{C,n-1}}{f}$$

$$= \zeta_{n-1,0,k}\frac{W_{C,n}}{f^2} + \zeta_{n-1,1,k}\frac{W_{C,n-1}}{f}$$

where

$$\zeta_{n-1,0,k} = g_{n-1,k}\left(\sum_p \chi_p g_{n,p}\right)$$

$$\zeta_{n-1,1,k} = g_{n-1,k}$$

are the portions of gate size set by the output load and the global wire capacitance, respectively.

In general, the size of any gate k in stage i can be expressed as

$$W_{i,k} = \sum_{j=i}^{n} \zeta_{i,n-j,k}\frac{W_{C,j}}{f^{n+1-j}} \tag{14.i}$$

The $\zeta_{i,n-j,k}$ terms are constant factors and computable for the given design.

In addition, note that the effect of output load or global wire capacitance $W_{C,j}$ on the gate size is reduced by the stage effort product of stages in between. That implies the effect of global wire capacitance to gates in preceding stages may outweigh that of the output load when large stage efforts are used.

The total delay of the datapath is

$$T_{d,Total} = \sum_{i=1}^{n}(f + p_i) \tag{15}$$

Using equation (d), the total energy is given by

$$E_{Total} = \sum_{i=1}^{n}\sum_{k} c_{g(i,k)} W_{g(i,k)} + E_{wire} \tag{16}$$

$$= \sum_{i=1}^{n}\sum_{k}\left(c_{g(i,k)}\sum_{j=i}^{n}\zeta_{i,n-j,k}\frac{W_{C,j}}{f^{n+1-j}}\right) + E_{wire}$$

$$= \sum_{i=1}^{n}\sum_{j=i}^{n}\left(\sum_{k} c_{g(i,k)}\zeta_{i,n-j,k}\frac{W_{C,j}}{f^{n+1-j}}\right) + E_{wire}$$

$$= \sum_{i=1}^{n}\sum_{j=i}^{n} E_{i,n-j} + E_{wire}$$

where

$$E_{i,n-j} = \left(\sum_{k} c_{g(i,k)}\zeta_{i,n-j,k}\right)\frac{W_{C,j}}{f^{n+1-j}}$$

The energy term $E_{i,n-j}$ refers to the energy consumption for the gate in stage i that is influenced by the output load or global wire capacitance $W_{C,j}$.

To achieve more efficient energy, the stage effort of each stage is varied by a factor y_i. That is, $f_i = y_i f$. It can be shown that the new gate size is

$$W_{i,k}\{y\} = \sum_{j=i}^{n} \zeta_{i,n-j,k} \frac{W_{C,j}}{f^{n+1-j} \prod_{p=i}^{j} y_p} \quad \textbf{(17)}$$

The new total delay of the datapath is

$$T_{d,Total}\{y\} = \sum_{i=1}^{n} (y_i f + p_i) \quad \textbf{(18)}$$

To maintain the same delay, it is necessary that

$$\sum_{i=1}^{n} y_i - n = 0 : \text{equal-delay constraint C} \quad \textbf{(19)}$$

Note that from (19) and $f_i > 0$ (i=1→n), the range of each y_i is (0, n).

The corresponding total energy is

$$E_{Total}\{y\} \quad \textbf{(20)}$$
$$= \sum_{i=0}^{n} \sum_{j=i}^{n} \sum_{k} c_{g(i,k)} \zeta_{i,n-j,k} \frac{W_{C,j}}{f^{n+1-j} \prod_{p=i}^{j} y_p} + E_{wire}$$
$$= \sum_{i=0}^{n} \sum_{j=i}^{n} \frac{E_{i,n-j}}{\prod_{p=i}^{j} y_p} + E_{wire}$$

The optimal energy can be found by solving the LaGrange function

$$F = \lambda C + E_{Total} \quad \textbf{(21)}$$
$$= \lambda \left(\sum_{i=1}^{n} y_i - n \right) + \sum_{i=1}^{n} \sum_{j=i}^{n} \frac{E_{i,n-j}}{\prod_{p=i}^{j} y_p}$$

The solution is obtained from (19) and n derivatives, $\partial F / \partial y_i = 0$ for i=1→n. The n derivatives can be simplified into

$$\lambda - \frac{1}{y_1} \sum_{j=1}^{n} \frac{E_{1,n-j}}{\prod_{p=1}^{j} y_p} = 0 \quad \textbf{(22.1)}$$

$$(y_2 - y_1) \sum_{j=2}^{n} \frac{E_{1,n-j}}{\prod_{p=1}^{j} y_p} + y_2 \frac{E_{1,n-1}}{y_1} = y_1 \sum_{j=2}^{n} \frac{E_{2,n-j}}{\prod_{p=2}^{j} y_p} \quad \textbf{(22.2)}$$

$$(y_3 - y_2) \sum_{i=1}^{2} \sum_{j=3}^{n} \frac{E_{i,n-j}}{\prod_{p=i}^{j} y_p} + y_3 \sum_{i=1}^{2} \frac{E_{i,n-2}}{\prod_{p=i}^{2} y_p} = y_2 \sum_{j=3}^{n} \frac{E_{3,n-j}}{\prod_{p=3}^{j} y_p} \quad \textbf{(22.3)}$$

(…)

$$(y_n - y_{n-1}) \sum_{i=1}^{n-1} \frac{E_{i,0}}{\prod_{p=i}^{n} y_p} + y_n \sum_{i=1}^{n-1} \frac{E_{i,1}}{\prod_{p=i}^{n-1} y_p} = y_{n-1} \frac{E_{n,0}}{y_n} \quad \textbf{(22.n)}$$

Equations (19) and (22.1)–(22.n) are solvable, using the numerical method. The run time remains O(n) where N is the number of stages.