ENERGY ESTIMATION OF CIRCUITS

From the model discussed in the earlier section, the energy consumption at a gate is

$$E_{gate} = \beta(E_p W_{in} + E_g W_{load}) \quad (a)$$

where

β : switching factor of the gate;

W_{in} : referenced input width;

W_{load} : equivalent gate width of output load.

Note that W_{load} may consist of the input width W_g of driven gates or the equivalent witdth W_w of the wire capacitance from the output to the furthest driven gate. That is,

$$W_{load} = \sum_p \chi_p W_{g,p} + W_w \quad (b)$$

where χ_p is the size factor relative to the reference input width W_g of gate p. The size factors for some CMOS gates are shown in Table 1. The PMOS-to-NMOS ratio of 2.5 is assumed.

Table 1. Size factors of CMOS gates

Gate	Ref. Input	Input	χ
INV NAND2 NOR2	any	any	1
AOI	and-input	and-input or-input	1 0.86
OAI	or-input	or-input and-input	1 0.64

The total energy consumed in a circuit is the summation of energy consumed in each of its gates.

$$E_{Total} = \sum_{i,j} E_{(i,j)} \quad (c)$$

where (i,j) refers to gate i in stage j. Using the expressions (a) and (b), the expanded form of energy is found.

$$\begin{aligned} E_{Total} &= \sum_{i,j} \beta_{(i,j)} [E_{p(i,j)} W_{g(i,j)} + E_{g(i,j)} W_{load(i,j)}] \\ &= \sum_{i,j} \beta_{(i,j)} [E_{p(i,j)} W_{g(i,j)} \\ &\qquad + E_{g(i,j)} (\sum_p \chi_{(p,k,l)} W_{g(k,l)} + W_{w(i,j)})] \\ &= \sum_{i,j} \beta_{(i,j)} [E_{p(i,j)} W_{g(i,j)} + E_{g(i,j)} \sum_p \chi_{(p,k,l)} W_{g(k,l)}] \\ &\qquad + \sum_{i,j} \beta_{(i,j)} E_{g(i,j)} W_{w(i,j)} \\ &= \sum_{i,j} \beta_{(i,j)} [E_{p(i,j)} + \sum_p \chi_{(p,i,j)} E_{g(k',l')}] W_{g(i,j)} \\ &\qquad + \sum_{i,j} \beta_{(i,j)} E_{g(i,j)} W_{w(i,j)} \end{aligned}$$

$$E_{Total} = \sum_{i,j} c_{g(i,j)} W_{g(i,j)} + \sum_{i,j} c_{w(i,j)} W_{w(i,j)} \quad (d)$$

where

$$c_{g(i,j)} = \beta_{(i,j)} [E_{p(i,j)} + \sum_p \chi_{(p,i,j)} E_{g(k',l')}]$$

$$c_{w(i,j)} = \beta_{(i,j)} E_{g(i,j)}$$

are constant factors. In addition, note that the 1st term depends only on the gate capacitance whereas the 2nd term depends only on wire capacitance and is mostly constant for a given design.