Design and Optimization of Sense Amplifier-Based Flip-Flops

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Abstract

An improved design of a sense amplifier-based flip-flop is presented. The new design overcomes the problems of floating nodes, which is a weakness of previously reported solutions. This is achieved by systematic derivation of flip-flop equations and rearranging the resulting network. The resulting flip-flop outperforms earlier published structures, exhibiting T_{CQ} of 190ps when driving 100fF load in a 0.18μm CMOS technology.

1. Introduction

Sense Amplifier based Flip-Flops (SAFF) have been used in high-performance and low-power digital systems. Recently reported modifications of SAFFs exhibit very small delay, calculated as a sum of setup time and clock to output delay in high-speed datapath applications. They have differential outputs, can be used with single or differential inputs and present a small clock load [1,2,3].

The initial design of a SAFF was based on the sense amplifier in the first and the NAND-based cross-coupled RS latch in the second stage, Figure 1 [1].

Modified SAFF improves the output stage to reduce the overall delay [3].

2. Analysis of Operation

The sense amplifier stage [1] is precharged during the interval when clock signal is low, generating falling transition after clock rises on only one of its outputs, $\overline{S}$ or $\overline{R}$. As reported in [1], SAFF did not include the transistor M_{N5}. Outputs of the first stage are incompletely defined logic functions, with NMOS pull-down trees implementing $\overline{S} = \overline{Clk \cdot \overline{R'} \cdot D}$, $\overline{R} = \overline{Clk \cdot \overline{S'} \cdot \overline{D}}$ functions and PMOS pull-up trees implementing $\overline{S} = \overline{Clk \cdot \overline{R'}}$, $\overline{R} = \overline{Clk \cdot \overline{S'}}$, represented by Karnaugh maps shown in Figure 2.a and Figure 2.b. $\overline{S'}$ and $\overline{R'}$ represent previous values of signals $\overline{S}$ and $\overline{R}$.

Values marked as "don't cares" (x) in Figure 2, actually represent floating outputs of the logic function, that are neither forced to 0 nor to V_{DD}. Essentially, the truth table includes four more don't cares, since both $\overline{S}$ and $\overline{R}$ can not be zero at the same time.

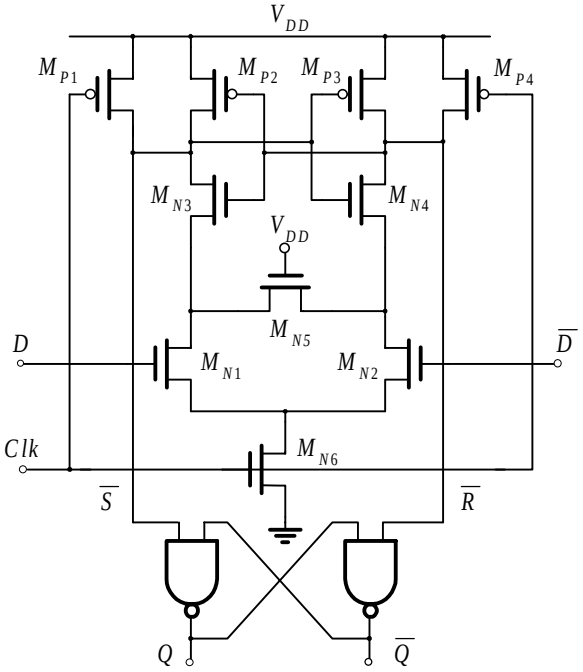


Figure 1: Sense amplifier-based flip-flop.

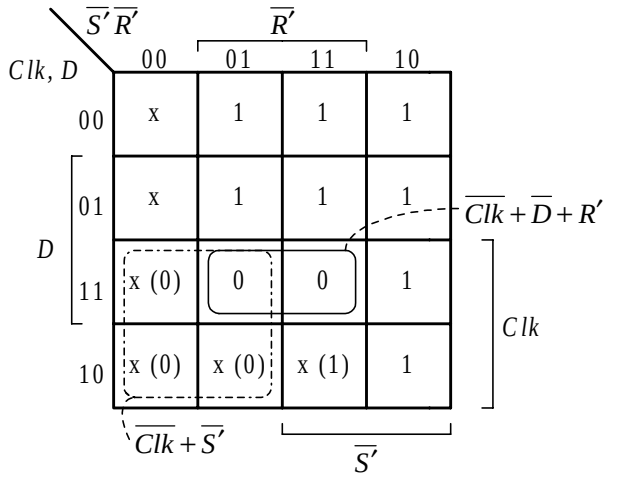
Ideally, when *Clk* is changing from 0 to 1, and *D* = 0, the value of the $\overline{S}$ node should remain unchanged, as well as the value of the node $\overline{R}$ when *Clk* is rising and *D* = 1.

The consequences of having don't cares in the Karnaugh map are explained in the case of $\overline{R}$:

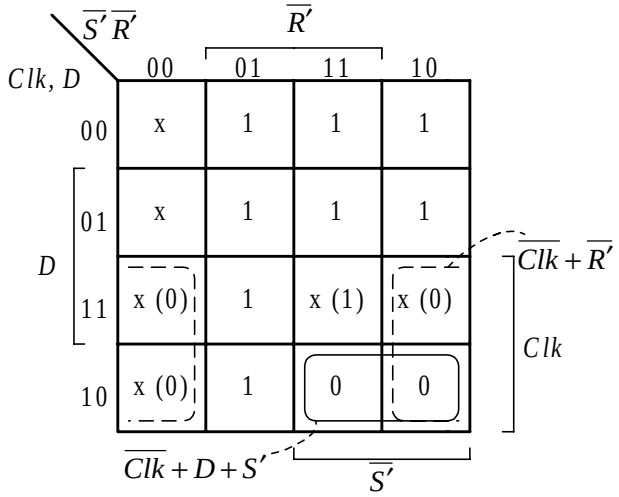
(a) *Clk* = 1, *D* = 1, $\overline{R'}$ = 1: This Karnaugh map entry is exercised when *Clk* changes from low to high logic level, causing the triggering of the flip-flop. With *D* being high, branch evaluating $\overline{S}$ is being pulled to low logic level, $\overline{R}$ floats, causing a glitch, (Figure 5) and slowing down the transition. Elimination of this situation would involve addition of another parallel pull-up PMOS branch, leading to diminishing returns in terms of speed. Because of this 'don't care' the new value of $\overline{R}$ is not forced directly by the branch evaluating it, but indirectly through the change of $\overline{S}$.

(b) *Clk* = 1, *D* = 0, $\overline{R'}$ = 0: This value corresponds to the case of the sense amplifier output $\overline{R}$ being forced low at the leading edge of the clock. If the data changes after the leading edge of the clock, leakage currents could charge this node, and eventually change the state of the flip-flop.

This problem was noticed in [2], and proposed modification is shown in Fig. 1. Additional transistor, M_{N5}, in Figure 1, allows static operation, providing a path to ground even after the data changes. This prevents eventual charging of the low sense-amplifier output, due to leakage currents, to the value when it could trigger the latch. This solution has two major disadvantages: a) the glitch on $\overline{S}$ is more emphasized due to the conducting path through M_{N5}, Figure 5; b) direct gate connection to long metal lines (V_{DD} or ground) is prohibited. This is due to very small gate thickness in deep-submicron technologies.



a)



b)

Figure 2: Karnaugh maps for a) $\overline{S}$, b) $\overline{R}$.

3. Flip-Flop Optimization

This problem can be solved in a more consistent way, by covering the Karnaugh maps as shown in Figure 2:

$$\overline{S} = Clk \cdot \overline{R'} \cdot \overline{\overline{D} \cdot \overline{S'}}, \qquad \overline{R} = Clk \cdot \overline{S'} \cdot \overline{D \cdot \overline{R'}}.$$

This modification involves addition of one NMOS transistor per each pull-down tree. Since the implementation of the SAFF as shown in [3], already includes the signals *S* and *R*, the gates of added transistors are connected to existing inverter outputs, so their addition does not change the input loading, and reduces the glitch magnitude. Additional inverters are used to decouple the loading of critical nodes $\overline{S}$ and $\overline{R}$ by transistor M_{N3} and M_{N4} gates [4], speeding up the flip-flop operation.

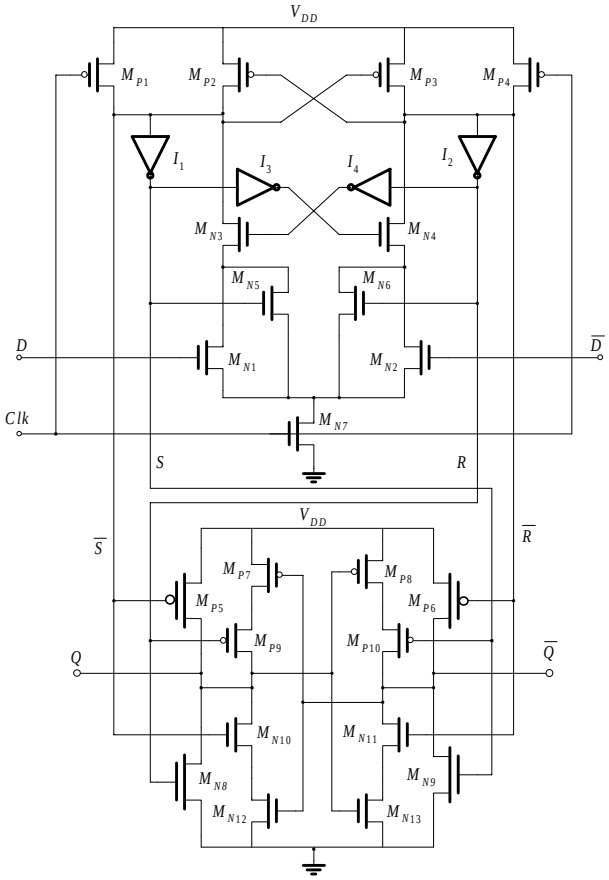


Figure 3: Modified sense amplifier-based flip-flop.

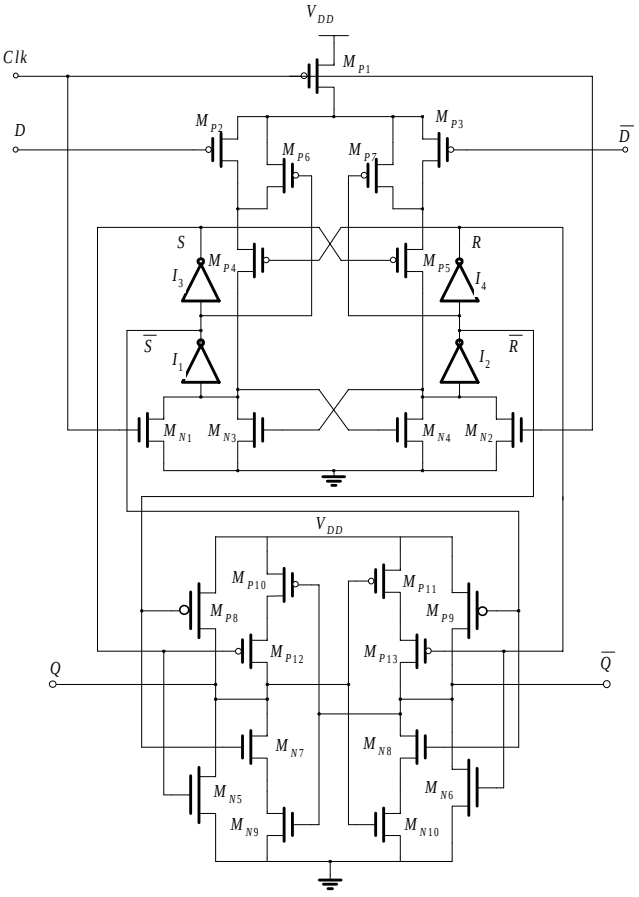


Fig. 4: Falling edge-triggered flip-flop.

4. Results

In addition to reliability improvement, proposed modification of the SAFF shows 5-10% faster operation over the design with cross transistor [2], as shown in Figure 6. This flip-flop was designed in 0.18μm L_{eff} CMOS, with improved output stage [3], optimized to drive the loads between 100 and 150fF. Clock to output delay is 190ps when driving 100fF load at both outputs. It is possible to design the falling edge-triggered SAFF with the same driving capability, Fig. 4. This flip-flop has the same setup time of –20ps and its delay characteristic is equidistant to the characteristic of the rising edge SAFF, with clock to output delay of 240ps when driving 100fF load. This is not the case with originally proposed design, based on cross-coupled NOR gates [1,2]. The results from Fig. 6 are obtained with the same size of the transistors in the output stage [3]. Two lines for SAFFs from [1] in Fig. 6, represent the cases when *i*) only one or *ii*) both outputs are loaded. Improved output stage design [3] has equal delays for both outputs, that is independent of the load on the other output.

5. Conclusion

A new design of sense-amplifier-based flip-flop is presented that eliminates floating nodes in the sense amplifier stage. By using the decoupling inverters the modification also results in improved switching speed. In addition the falling edge flip-flop was designed with equidistant characteristic of delay vs. load.

References

[1] M. Matsui *et al*. "A 200MHz 13mm2 2-D DCT Macrocell Using Sense-Amplifying Pipeline Flip-Flop Scheme," IEEE Journal of Solid-State Circuit, vol. 29, no. 12, pp. 1482-1490, Dec. 1994.

[2] D. Dobberpuhl, "The Design of a High Performance Low Power Microprocessor," Proceedings International Symposium on Low-Power Electronics and Design, August 1996.

[3] B. Nikolic *et al* "Sense Amplifier-Based Flip-Flop," 1999. International Solid-State Circuits Conference, Digest of Technical Papers, February 1999.

[4] F. Klass, "Semi-Dynamic and Dynamic Flip-Flops with Embedded Logic," Symposium on VLSI Circuits, Digest of Technical Papers, June 1998.

[5] V. Stojanovic, V.G. Oklobdzija, "Comparative Analysis of Master-Slave Latches and Flip-Flops for High-Performance and Low-Power Systems," IEEE Journal of Solid-State Circuits, vol. 34, no. 4, pp. 536-548, April 1999.

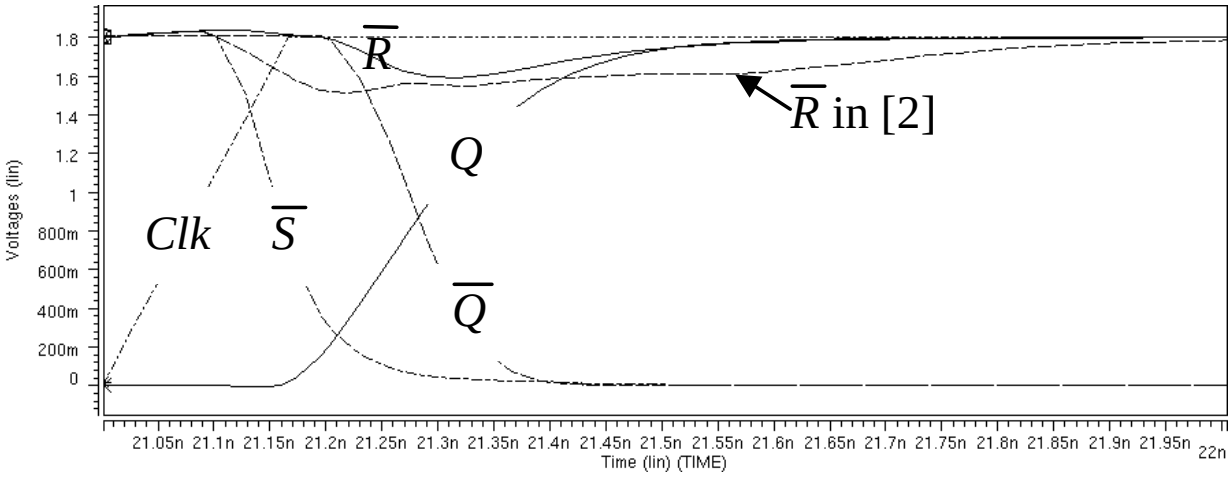


Fig. 5: Typical SAFF waveforms.

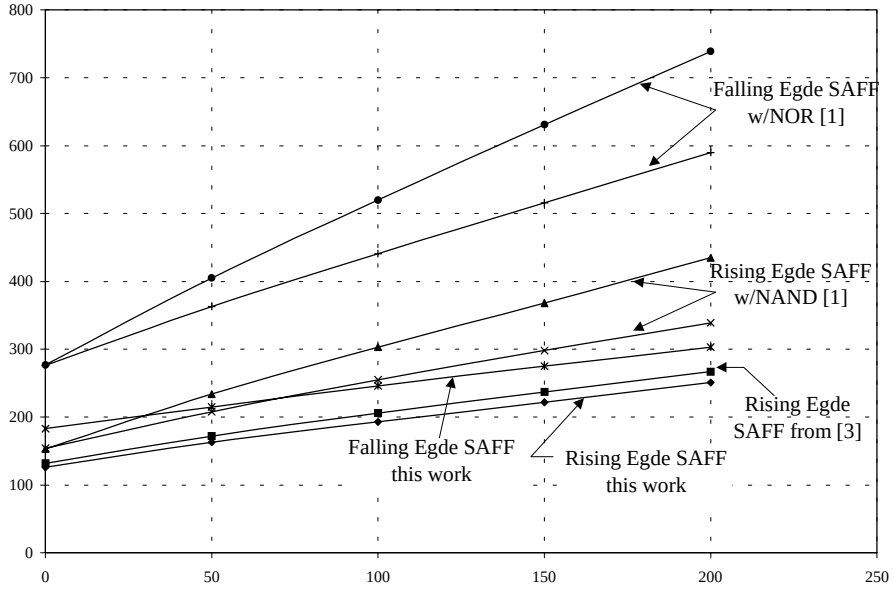


Fig. 6: Delay vs. load for different SAFFs.