Estimating the Power Consumption of CMOS Adders

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Abstract

Minimizing the power consumption of circuits is important for a wide variety of applications, both because of the increasing levels of integration and the desire for portability. Since adders are so widely used in computers, it is also important to maximize the speed. Frequently, the compromise between these two conflicting demands is accomplished by minimizing the product of the power consumption and the delay. This paper reports on the dynamic power dissipation and speed of CMOS implementations of six different adders. Simulation and direct measurement of the performance of a test chip were used to evaluate their switching characteristics, and the results are used to rank the adders on speed, size, and dynamic power dissipation.

1 Introduction

An important attribute of arithmetic circuits for most applications is maximizing the speed or throughput. For a growing number of applications, minimizing the power consumption is of equal or greater importance. The most direct way to reduce the power is to use CMOS circuits, which generally dissipate less power than their bipolar counterparts. Even for CMOS, the use of adders with minimum power consumption is attractive to increase battery life in portable computers, to avoid local areas of high power dissipation which may cause hot spots, and to reduce the need for a low impedance power and ground distribution network which may interfere with signal interconnections.

In static CMOS the dynamic power dissipation of a circuit depends primarily on the number of logic transitions per unit time [1]. As a result, the average number of logic transitions per addition can serve as the basis for comparing the efficiency of a variety of adder designs. If two adders require roughly the same amount of time and roughly the same number of gates, the circuit which requires fewer logic transitions is more desirable as it will require less dynamic power.

Previous attempts to estimate energy consumption (dissipation) for VLSI circuits have included attempts to estimate the worst-case energy consumption for general circuits. Kissin [2] calculated worst-case upper and lower bounds of acyclic circuits built out of 2-input AND and OR gates, and inverters where power is consumed by the wires connecting gates as well as the gates themselves. Cirit [3] attempts to measure the average power dissipation of CMOS circuits under a wide range of operating conditions by using statistical methods to calculate the probability that a gate will switch states. Jagau [4] attempts to find the worst-case power dissipation of static CMOS circuits by combining a logic simulator with results from the analog simulation of two switching reference gates. More recently, Callaway and Swartzlander have investigated the average power dissipation of adders [5] and multipliers [6]. Devadas, *et al* [7] have attempted to estimate the maximum power dissipation of CMOS circuits using boolean function manipulation combined with a simple gate model.

The results presented in this paper were obtained from three different sources. A gate level simulator was used to generate a first estimate of each adder's dynamic power consumption. For that gate level simulator, the adders are constructed using only AND, OR, and INVERT gates. The circuits are then subjected to a user-specified number of pseudo-random inputs. For each input, the number of gates that switched during the addition is counted and.

The second estimate is derived from detailed circuit simulation using a program called CAzM, which is similar in behavior to SPICE. A 16 bit version of each adder was designed in 2 micron static CMOS using MAGIC, and the resulting layout was the basis for the circuit simulation. Transistor parameters are those of a recent 2 micron MOSIS fabrication run.

Each adder is presented with 1,000 pseudo-random inputs, and the average power supply current waveform is plotted. Each addition is allowed a time of 100 nanoseconds, so that the voltages will stabilize completely before the next addition is performed. Since the worst case delay of the longest adder is approximately 55 nsec, this provides adequate time for the circuits to stabilize.

The third method for obtaining results relies on direct physical measurement. A chip has been designed, fabricated, and tested, containing 16 bit implementations of the six different adders. Each of the six adders has its own power pin, which enables direct measurement of each adder's dynamic power dissipation without having to estimate other power sinks.

The resulting chip occupies an area of 6400 x 4800 square microns, and has 65 pins. There are 33 adder input pins (16 bits + 16 bits + 1 carry in), 17 adder output pins (16 bits + 1 carry out), 3 multiplexer control pins (an 8:1 mux is used to select either one

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of the six adder outputs or either of the 2 inputs), 6 adder power pins, 1 mux power pin, 1 adder and mux ground pin, and 2 power and 2 ground pins for the pads.

2 Adder Types

The following types of adders were simulated: Ripple Carry [8], Constant Block Width Single-level Carry Skip [8], Variable Block Width Multi-level Carry Skip [12], Carry Lookahead [9], Carry Select [10], and Conditional Sum [11].

In choosing an adder for a particular application, several things must be considered, including speed, size, and dynamic power consumption. The speed is usually considered to be the worst case number of gate delays from input to the slowest output (typically the most significant sum bit). Table 1 presents the worst case number of gate delays for the six adders For the purposes of this paper, all gates are assumed to have the same delay, regardless of the fan-in or fanout.

Table 1: Worst Case Delay

Adder Type	Adder Size		
	16	32	64
Ripple Carry	36	68	132
Constant Width Carry Skip	23	33	39
Variable Width Carry Skip	17	19	23
Carry Lookahead	10	14	14
Carry Select	14	14	14
Conditional Sum	12	15	18

The size of each adder is approximated to a first order by the number of gates, which is given in Table 2. The actual area required for a given adder will depend on the types of gates (i.e., three or four input gates require more area than two input gates), the amount of wiring area, and the available form factor, as will be seen in the next section.

Table 2: Number of Gates

Adder Type	Adder Size		
	16	32	64
Ripple Carry	144	288	576
Constant Width Carry Skip	156	304	608
Variable Width Carry Skip	170	350	695
Carry Lookahead	200	401	808
Carry Select	284	597	1228
Conditional Sum	368	857	1938

3 Gate Level Simulation

The gate-level simulator used to measure the average number of gates that switch during an addition accepts as its input a linked list of gates, with each gate pointing to its inputs, and also the next gate to be evaluated. The circuits themselves are built in C subroutines, and a pointer to the first gate in the circuit is passed to the simulator. The circuits then perform a user-specified number of additions with pseudo-random input patterns. For each pattern, the number of gates that switch during the addition is counted.

Before the first pseudo-random pattern is applied, the adder is initialized by applying zero inputs and allowing it to stabilize. Any gate transitions during this initialization are not counted. After that, pseudo-random inputs are presented one after the other, with no zero inputs in between. This is analogous to the adder being used in a vector processor with a vector length of 50,000. Table 3 gives the average number of transitions per addition observed for each adder in 50,000 randomly distributed input patterns with a random distribution of carry inputs.

Table 3: Average Number of Logic Transitions

Adder Type	Adder Size		
	16	32	64
Ripple Carry	90	182	366
Constant Width Carry Skip	102	199	392
Variable Width Carry Skip	108	220	437
Carry Lookahead	100	202	405
Carry Select	161	344	711
Conditional Sum	218	543	1323

Figures 1, 2, and 3 show the probability distributions of the number of gate transitions for the six different adders based on the simulations with 50,000 input patterns.

4 Circuit Simulation Results

The simulator used to obtain the results in the previous section uses a rather simple model, and provides no time information. In order to verify those results, 16 bit versions of the six different adders were custom designed in 2 micron CMOS using Magic. Netlists were extracted from the layout, and the CAzM circuit simulator was then used to estimate the worst case delay and the average power dissipation.

Table 4 shows the worst case delay of the six adders as estimated with CAzM. This delay was obtained by setting all of the inputs to zero initially, and then changing the carry in and one of the inputs words to all ones. The delay is then the length of time that the circuit takes to stabilize. The table also shows an approximate delay based on the delays in Table 1 with $\Delta = 1.45$ nsec. The delay from CAzM for the constant block width carry skip adder is about 15% faster than estimated by the "unit delay" model, while the CAzM delay estimates for the carry lookahead and the carry select adders are about 20% to 25% slower than predicted by the unit delay model. In the case of the carry lookahead adder, the greater delay is probably due to its use of three and four input gates and a fan out of greater than two in the carry lookahead logic. For the conditional sum adder, the greater delay is probably due to the long path lengths.

Table 5 shows the area occupied by each adder in mm^2 and number of gates. The areas indicated in Table 5 exhibit a wider range (approximately 6:1) than the gates counts from Table 2 (range of approximately 2.5:1), but the relative sizes are consistent with the gate counts. Part of the explanation for the wider range in sizes is that the ripple carry adder is laid

Table 4: Worst Case Delay Estimated with CAzM

Type of adder	Delay (nsec)	$\Delta = 1.45$ nsec	error
Ripple Carry	54.27	52.2	-2.1
Constant Width Carry Skip	28.38	33.3	4.9
Variable Width Carry Skip	21.84	24.6	2.8
Carry Lookahead	17.13	14.5	-2.6
Carry Select	19.56	20.3	0.7
Conditional Sum	20.05	17.4	-2.7

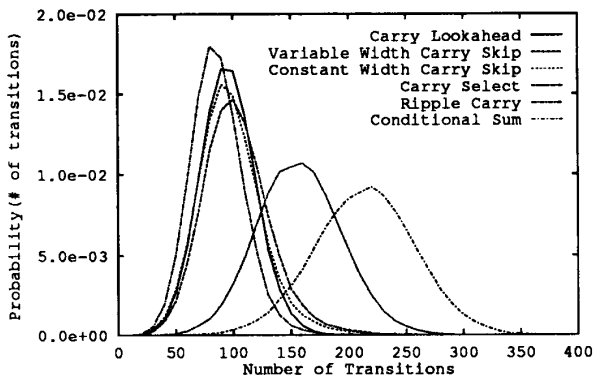

Figure 1: 16 Bit Adder Logic Transition Histogram

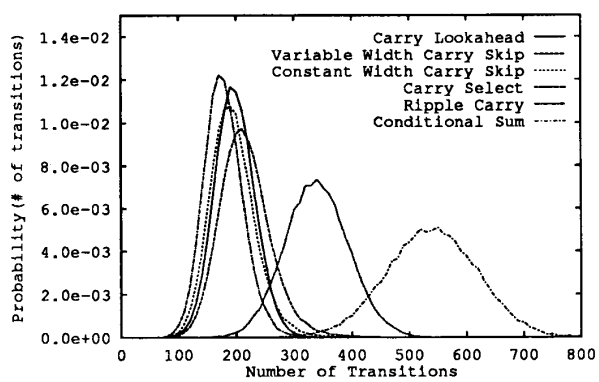

Figure 2: 32 Bit Adder Logic Transition Histogram

out in a single row, while all of the others require multiple rows with varying amounts of "wasted space" for signal routing between the rows. With additional effort, the larger adders (i.e., carry lookahead, carry select, and conditional sum) could be laid out more compactly.

Table 5: Adder Area

Type of Adder	Size	Count
Ripple Carry	0.2527	144
Constant Width Carry Skip	0.4492	156
Variable Width Carry Skip	0.5149	170
Carry Lookahead	0.7454	200
Carry Select	1.0532	284
Conditional Sum	1.4784	368

The average power dissipation per addition shown in Table 6 is obtained by simulating the addition of 1,000 pseudo-random inputs, and averaging the results. The average power dissipation is lower for the constant width carry skip adder than for the ripple carry adder because the power supply current falls to zero faster, even though it is larger at the peak for the constant width carry skip adder.

Table 6: Average Power Dissipation with CAzM

Type of Adder	Power (Watts)
Ripple Carry	1.17
Constant Width Carry Skip	1.09
Variable Width Carry Skip	1.26
Carry Lookahead	1.71
Carry Select	2.16
Conditional Sum	3.04

Because CAzM also provides timing information, it is useful to look at the distribution in time of the average power dissipation. This easily done by storing the curve of power supply current versus time for each individual addition. Then after all 1,000 additions, the curves are averaged together. This one curve then represents the average power dissipation (power supply current times power supply voltage) with respect to time of the adder, as shown in Figure 4 for each of the six adders.

5 Physical Measurement

The third method of obtaining results is to directly measure the power dissipation. The test chip shown in Figure 5 was constructed so that each adder has

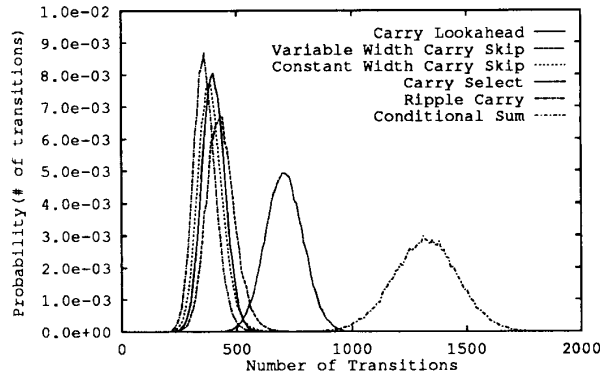

Figure 3: 64 Bit Adder Logic Transition Histogram

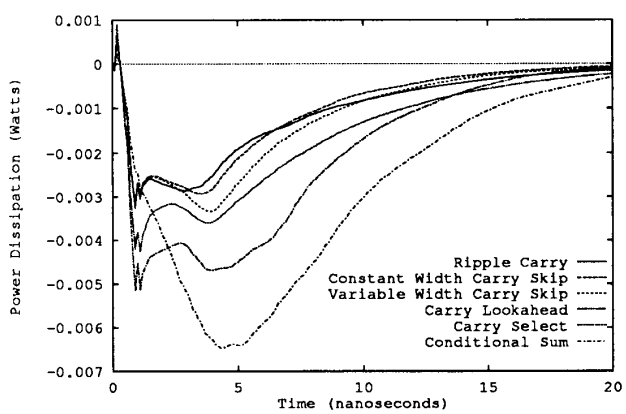

Figure 4: Average Power Dissipation with CAzM

Table 7: Average Measured Power Supply Current

Type of Adder	Current (μA)
Ripple Carry	85.7
Constant Width Carry Skip	98.1
Variable Width Carry Skip	99.3
Carry Lookahead	115.8
Carry Select	138.2
Conditional Sum	167.0

a separate power pin. Only the pads and the output multiplexer share a power net. There is a common ground for all devices.

All six of the adders in Figure 5 are contained in the center of the chip. The adders run horizontally, and are laid out from top to bottom in the same order as in the tables, i.e. the topmost adder is the ripple carry adder, and the bottommost adder is the conditional sum adder. The vertical row of cells to the left of the adders is a 17-bit wide 8:1 output multiplexor.

Because each adder has its own power pin, measuring the power dissipation is simple. The mux is set to select the correct adder output for test purposes, and two power supplies are connected, one for the pads and the mux, and one for the adder. A simple test board was constructed to provide inputs and functionality testing for the chips. Linear Feedback Shift Registers on the test board were used to generate the pseudo-random operands, and a separate adder on the test board was used to verify that the adders were functional at the 2 MHz clock rate of the test board.

The power supply current was measured by inserting a 100 Ω resistor in series with the power supply, and a small (about 1 nanofarad) bypass capacitor to provide some spike filtering. The power supply current can then be determined by measuring the voltage across the resistor. A Tektronix TDS 460 digital Oscilloscope was used to collect and average the voltage across that resistor over a moving window of 1,000 additions. Figures 6–11 show photos of the average voltage across that 100 Ω resistor for the six different adders at a clock frequency of 2 MHz.

As seen in the scope photos in Figures 6–11, the test board adds quite a bit of delay. The power supply current indicates that the operands are not even received by the adder inputs until about 50 nsec have passed. The long tail of the power supply current is most likely due to the oscilloscope being set for 20 MHz bandlimiting.

Another set of measurements was made by connecting a multimeter in series with the power supply and measuring the current while the adders are accepting pseudo-random inputs. The average current drawn by each adder is presented in Table 7. The problem with this measurement is that it is difficult to tell exactly what period of time the multimeter is measuring the current over. These measurements are in close agreement with the results from the simple gate level model and the results from CAzM.

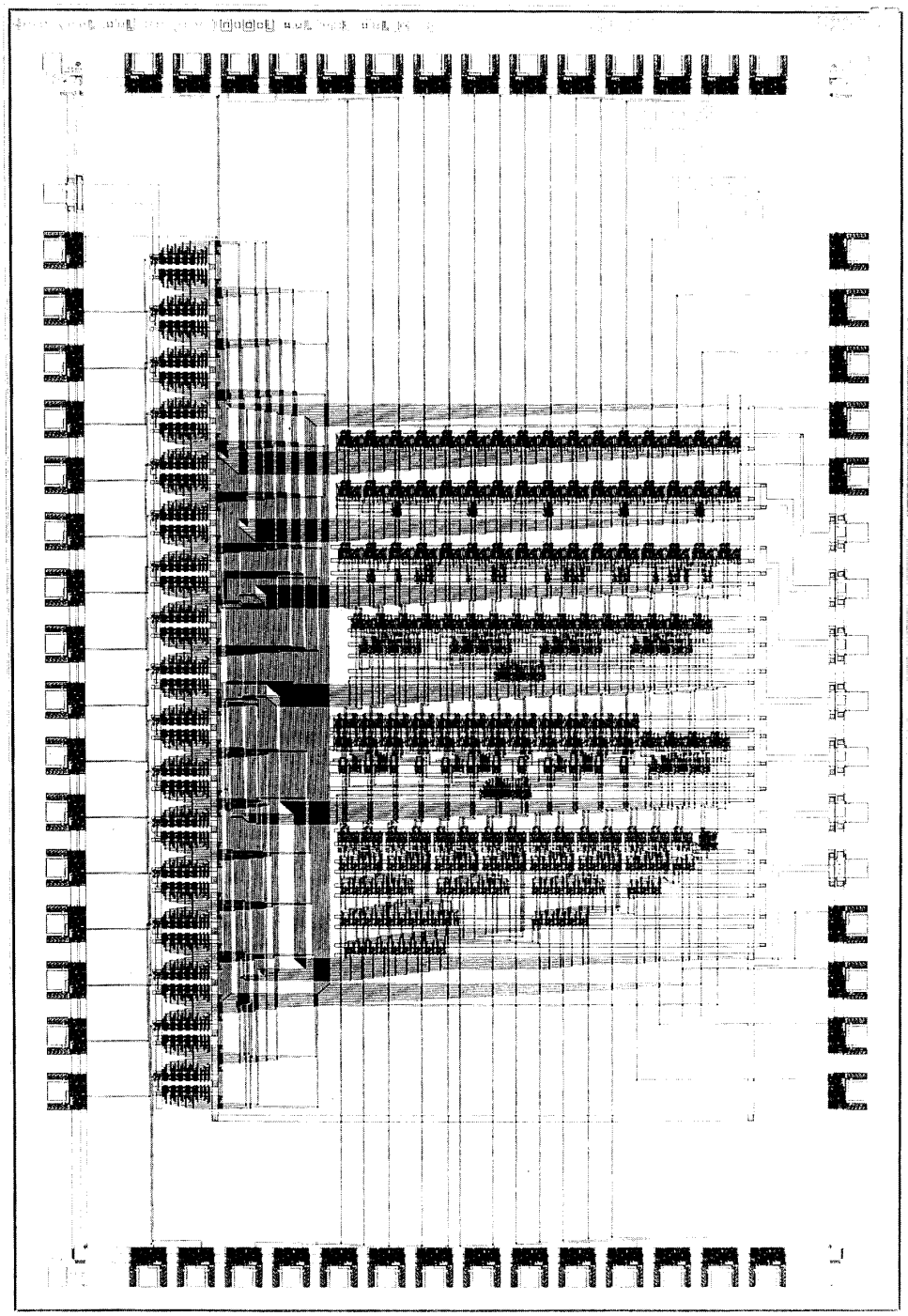

Figure 5: Die Photo of Test Chip.

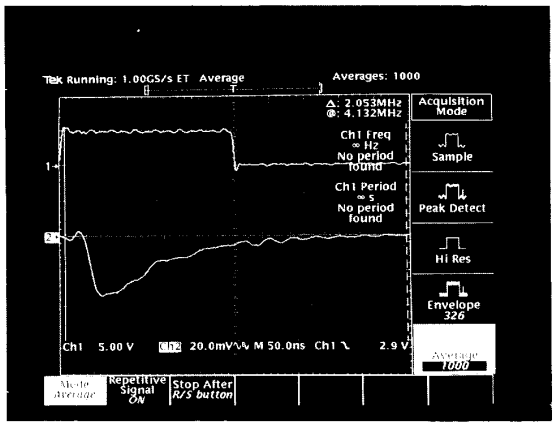

Figure 6: Ripple Carry Adder.

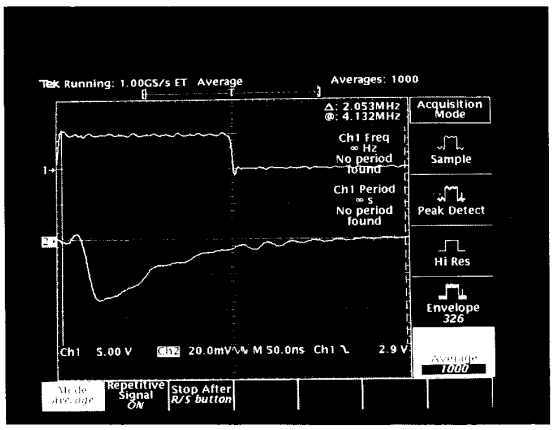

Figure 7: Constant Width Carry Skip Adder.

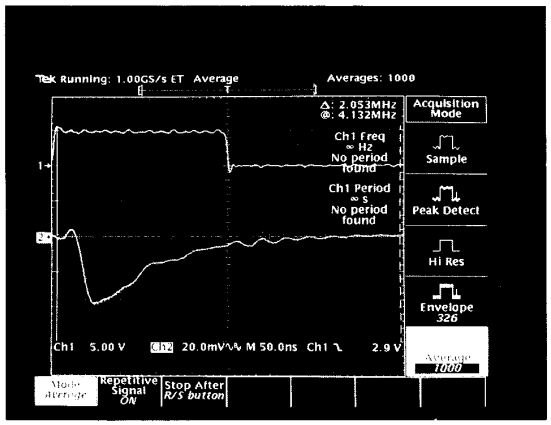

Figure 8: Variable Width Carry Skip Adder.

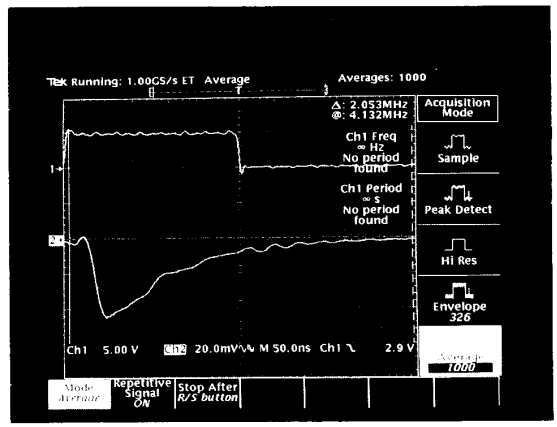

Figure 9: Carry Lookahead Adder.

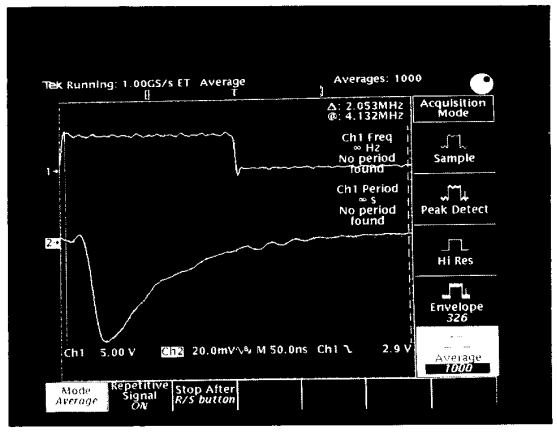

Figure 10: Carry Select Adder.

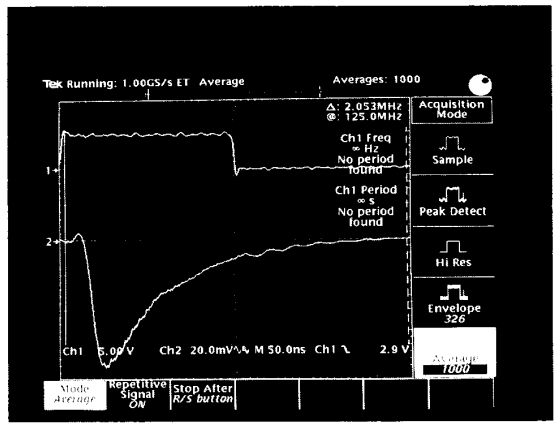

Figure 11: Conditional Sum Adder.

6 Conclusions

In this paper we have examined 6 types of adders in an attempt to model their power dissipation. We have shown that the use of a relatively simple model provides results which are qualitatively accurate, when compared to more sophisticated models, and to physical implementations of the circuits.

The main discrepancy between the simple model and the physical measurements seems to be the assumption that all gates will consume the same amount of power when they switch, regardless of their fan-in or fanout. Because the carry lookahead adder has several gates with a fanout and fan-in higher than 2, the simple model under estimates its power dissipation. The next step in this research is the development of a more accurate gate-level model which will include the ability to provide timing information and will model the power dissipation of each gate according to its fan-in and fanout.

Acknowledgements

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References

[1] N. Weste and K. Eshraghian, *Principles of CMOS VLSI Design: A Systems Perspective*, Addison-Wesley Publishing Company, 1988.

[2] G. Kissin, "Measuring Energy Consumption in VLSI Circuits: A Foundation," *Proceedings of the 14th ACM Symposium on the Theory of Computing*, pp. 99–104, 1982.

[3] M. Cirit, "Estimating Dynamic Power Consumption of CMOS Circuits," *ICCAD*, pages 534–537, 1987.

[4] U. Jagau, "SIMCURRENT - An Efficient Program for the Estimation of the Current Flow of Complex CMOS Circuits," *DAC*, pp. 396–399, 1990.

[5] T. K. Callaway and E. E. Swartzlander, Jr., "Optimizing Adders for WSI," In *IEEE International Conference on Wafer Scale Integration*, pp. 251–260, 1992.

[6] T. K. Callaway and E. E. Swartzlander, Jr., "Optimizing Arithmetic Elements for Signal Processing," *VLSI Signal Processing, V*, pp. 91–100, 1992.

[7] S. Devadas, K. Keutzer, and J. White, "Estimation of Power Dissipation in CMOS Combinational Circuits Using Boolean Function Manipulation," *IEEE Transactions on CAD*, vol. 11, pp. 373–380, 1992.

[8] D. Goldberg. "Computer Arithmetic," In D. A. Patterson and J. A. Hennessey, *Computer Architecture: A Quantitative Approach*, Morgan Kaufmann Publishers, 1990, pp. A2, A3, A31–A39.

[9] O. L. MacSorley, "High-Speed Arithmetic in Binary Computers," *IRE Proceedings*, vol. 49, pp. 67–91, 1961.

[10] O. J. Bedrij, "Carry-Select Adder," *IRE Transactions on Electronic Computers*, vol. EC-11, pp. 340–346, 1962.

[11] J. Sklansky, "Conditional-Sum Addition Logic," *IRE Transactions on Electronic Computers*, vol. EC-9, pp. 226–231, 1960.

[12] S. Turrini, "Optimal Group Distribution in Carry-Skip Adders," *Proceedings of the 9th Symposium on Computer Arithmetic*, pp. 96–103, 1989.

[13] P. K. Chan, *et al*, "Delay Optimization of Carry-Skip Adders and Block Carry-Lookahead Adders Using Multidimensional Dynamic Programming," *IEEE Transactions on Computers*, vol. EC-41, pp. 920–930, August 1992.