Tutorial:

Design of Power Efficient VLSI Arithmetic: Speed and Power Trade-offs

Given by:

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This tutorial will talk about issues related to performance of arithmetic algorithms when implemented in silicon. Most of the algorithms in use today are based on old and antiquated methods of counting the number of logic gates in the critical path. This produces inaccurate and misleading results. The importance of loading and wire delay is not taken into account by most. As the technology scales further into the sub-micron range, wire starts to dominate the delay. We will show how differed topologies of VLSI adders may influence fan-out and wiring density thus influencing design decisions and yielding to better area/power then known cases. This tutorial will further emphasize a disconnect that exists between algorithms that are used and the final result. The importance of accounting for Fan-In and Fan-Out on the critical path has been demonstrated in Logical Effort (LE) method which can be used for quick speed estimation. However, Logical Effort is not complete if the energy is treated separately. The power is starting to limit the speed of VLSI processors. But, even if we are able to manage the total power, the power density remains a problem.

In the course of VLSI processor design it is very important to choose the circuit topology that would yield desired performance for a given power budget. However, the performance and power of a chosen topology will be known only after the fact, i.e. after the design is finished. Therefore a question remains, could a higher performance have been achieved had a different topology been chosen? The answer is generally not known because there is no consistent nor realistic speed estimation method employed today.

We motivate the concept of comparing VLSI structures based on their energy-delay trade-offs and we discuss techniques used for estimating the energy-delay space of various high-performance VLSI topologies.

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