Foreword

We welcome you to the 17th IEEE Symposium on Computer Arithmetic, held in Hyannis, Cape Cod, Massachussetts, USA, June 27-29, 2005. The proceedings contain all the papers presented at the symposium as well as abstracts from the invited keynote talk, given by Prof. William Kahan, and abstracts for our two panel sessions on "Pain Versus Gain in the Hardware Design of FPUs and Supercomputers on a Chip," and "A Programmer's View of Computer Arithmetic and Standardization." This year's symposium is dedicated to Prof. William Kahan for his lifetime contributions to mathematics, numerical analysis, and standardization of computer arithmetic.

Since 1969, the ARITH symposium has been the conference for reporting new innovative techniques in the theory of arithmetic peformed in computers as well as detailing the design of new arithmetic units in state of the art microprocessors and embedded processors. The symposium is a biennial event and has been hosted in many countries including the recent ARITH-16 in Spain, and returns every other time to North America. The symposia is truely an international conference. The call for papers drew 86 submissions from 26 countries including several countries participating for the first time. Our program committee consists of 34 experts in computer arithmetic. Most of the reviews were done by three or more program committee members, and the members consulted with 54 external reviewers. The reviews were discussed at a Program Committee meeting in January 2005 in Fort Lauderdale, Florida by 22 members of the committee. Only 34 papers were approved for the symposium out of the 86 submissions.

This year's technical program includes 34 papers with authors representing 13 countries. There are 8 sessions presenting papers which include: "Multiplication," "Applications," "Addition," "Division," "Cryptography and Galios Fields," "Number Systems," and part 1 and 2 of "Function Evaluation and Table Methods." These paper detail state of the art techniques for computer arithmetic that are in use today or in the near future. For instance the Cell processor's SPU is detailed which will be used in future video game systems. Techniques for performing complex arithmetic functions such as inverse tangent on recently released microprocessors are shown. Advances have been made in basic operations such as adder design and in dual datapath fused multiply-adders. These papers, the panel sessions, and the keynote talk provide a spectrum of all the current research in computer arithmetic including both academic research and development in industry.

The success of the symposia depends on the contributions and involvement of many individuals. We would like to thank all the authors who submitted their latest research results to this symposia. We would also like to thank the Program Committee and the external reviewers for their time in providing detailed reviews of each submission. We would like to thank our webpage master, Fabrizio Lamberti who made submissions and organization easy. We would also like to thank the direction provided by the Steering Committee and the time and effort given by our financial and local arrangements chairs, Andrew Beaumont-Smith and Sri Samudrala, and our publicity chair, Elisardo Antelo. Finally we would like to thank the guidance provided by the General Chair, Israel Koren.

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Paolo Montuschi and **Eric Schwarz**
Program Chairs