Round Table:

Pain Versus Gain in the Hardware Design of FPUs and Supercomputers

Organized by:

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In 1990 there was a dramatic change in the overall design of floating-point units (FPUs) with the introduction of the fused multiply-add dataflow. This design is common today due to its performance advantage over separated units. Recently the constraining parameters have been changing for sub 10 micron technologies and the resulting designs are focusing on increasing the frequency at the cost of pipeline depth. Wire lengths are a crucial design parameter and there is a great deal of effort spent in floorplanning the execution elements to be very close together. It is now typical that a signal sent across an FPU may take 1 or more clock cycles. Thus, the physical design is very important and requires global optimizations of placement of macros as well as complex power reduction. Additionally technology scaling continues to decrease feature sizes and more execution units or even processor cores can be placed on a chip. Execution units such as Decimal FPUs are in product plans. There are single chip designs with 8 vector processing units which are used to accelerate the video games we play. The processing power in these single chip game processors is the equivalent of supercomputers. What is the next trendsetting design or key problem in computer arithmetic? We have asked a panel of expert arithmetic unit hardware designers to discuss the current pain versus gain tradeoffs and to speculate on the future of arithmetic design.

Panelists:

- Silvia Mueller, IBM Corp., Cell Processor Development
- Stuart Oberman, NVIDIA, Graphics Accelerators
- Martin Schmookler, IBM Corp., PowerPC and zSeries Floating-Point Unit Development
- Debjit DasSarma, AMD, Floating-Point Unit Development
- Andrew Beaumont-Smith, P.A. Semi, Low-Power Processor Design