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A Note on Conditional-Sum Addition for Base -2 Systems

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Abstract—**Conditional-sum addition in a -2 base system and its comparison with normal binary conditional-sum addition is discussed. It is found that approximately 2.0 to 2.5 times as much hardware is required for this high-speed addition method in the negative binary system as compared to the positive binary system.**

Index Terms—**Base -2 arithmetic, conditional-sum method, fast adder, negative radix.**

The principle of negative radix arithmetic has been used in several computers built in Poland [1]-[4]. Other investigations into negative radix systems deal primarily with the theory of fundamental arithmetic algorithms and conversion between positive and negative base representions [5]-[10]. No study has been reported in the literature, to the authors' knowledge, of fast-addition techniques (e.g., conditional-sum) in base -2 systems.

Negative radix representation results in a system that is indifferent to the sign of a number [10]. This can simplify algorithms involving operands of opposite signs. Further, it has been shown that base -2 coding can be useful in the design of systems with the requirements of variable word-length structure and modular construction [5].

References [11]-[13] discuss conditional-sum addition (CSA) in +2 base systems. For such systems, large gains in addition speed can be obtained as compared with the standard parallel addition (PA) technique. For the cases of operands of 12, 16, 32, and 48 bits, the ratio of PA to CSA addition times are approximately 2.4, 3.2, 5.0, and 6.9, respectively. Even greater speed gains are possible in the CSA case if more than one pair of operands can be processed in the adder at one time (pipelining). It is easy to show that essentially identical processing speeds can be obtained in negative base CSA systems, operating in either a regular or in a pipelined mode.

We now describe results of an investigation into CSA mechanization costs for negative binary systems; some interesting conclusions are shown in [13]. The following table contains the PA and CSA hardware requirements found necessary for 12, 16, 32, and 48-bit operands in positive and negative binary systems.

Hardware Requirements

Adder Type	Positive Binary NAND Gates				Negative Binary NAND Gates			
	$N = 12$	$N = 16$	$N = 32$	$N = 48$	$N = 12$	$N = 16$	$N = 32$	$N = 48$
Standard Parallel (Synchronous) Adder	108	144	288	432	144	192	384	576
Conditional-Sum Adder	216	289	655	1083	448	594	1447	2656

The number of gates (NAND gates were used exclusively in the design) for both types of adders are shown in the table. From these results we see the following.

1) Using the standard full-parallel adder, the logic is only slightly more in the negative binary system than in the positive binary system (about 33 percent more).

2) Increasing the speed of addition (by using the CSA instead of the PA method) increases the cost of hardware by a factor of about 2.0 to 2.5 in base +2 systems, and by roughly 3.0 to 4.5 in the base -2 case.

3) A CSA system in a -2 base representation requires approximately 2.0 to 2.5 times as much hardware as it does in a +2 base code.

It may be concluded that if a system is to be designed using PA-based arithmetic, the increase in adder cost due to the choice of -2 as a base seems small enough if the "flexibility" offered by the negative radix representation can be taken advantage of effectively. In the CSA case, the cost increase due to the choice of -2 as a base is even greater, and may or may not be justified on the basis of overall design goals. In any event, it is worth remembering that in a computer system, the cost of CPU logic represents only a small part (10 to 15 percent) of the total cost and with the greater use of LSI this figure is going to go downwards. Therefore, unless high-speed addition at lowest cost is the overriding criterion for design, the advantages of negative radix representation must be taken into account carefully before rejecting it.

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