# THE LOGIC OF MODULO 2k + 1 ADDERS

Ъv

Jean P. Chinal

#### Abstract

The design of modulo  $2^k + 1$  adders for arbitrary k is considered, with the objective of achieving a logic structure as regular as possible so as to allow a convenient implementation in large-scale integration technology (LSI). It is shown how the design problem can be reduced to the recursive generation of a subtract signal and to the merging, in various degrees, of the corresponding logic with the logic of an ordinary adder or, alternately, of a so-called signed-carry adder which is defined and designed itself in general, with both recursive and explicit carry schemes. Modulo  $2^k + 1$  adder designs explicit carry schemes. modulo 2 + 1 adder designs are given, one with conventional adder, another based on signed-carry adder and a third, derived from the signed-carry scheme, where subtract signal generation and carry logic are merged. This last scheme can be set up with two backward recursion chains and five or six forward ones. Two more basic variants are finally indicated for this integrated scheme, aiming at reducing as much as possible the residual logic structure irregularity presented by the most significant position in the word.

#### 1. Introduction

Modulo m adders are basic to error-coded arithmetic. for detection or correction of faults in digital processors, for operand or check word arithmetic 3,4,5 or for the design of residue generators 6. Also they are used in binary-coded residue class arithmetic 7,8. For multiple-residue error checking 8,9 and for residue class arithmetic it is necessary to implement modulo m addition for several distinct moduli having some mutual relationships such as being mutually prime 8. Moduli of the form 2 -1 or 2 +1 are often advocated, owing to the simplicity of their implementation. Both are very convenient for residue generation of an arbitrary binary number owing to the possibility of dividing the number in chunks of length k and using tree networks 6. Also modulus 2 -1 addition is closely related to double zero digit-complement addition 10,11,12 and is identical to non-overflowed, (single) negative-zero digit complement arithmetic 13.

Additionally, modulus 5 adders and generators appears in various hardwired binary to decimal schemes <sup>11</sup>, in BCD arithmetic <sup>11</sup> and modulus 9 comes into play for BCD arithmetic checking. Finally large moduli of the form 2<sup>K</sup>+1 may be used in conjunction with modulus 2<sup>K</sup>-1 in multiple checking or residue arithmetic <sup>8,9</sup> so as to provide pairs of moduli that would be at the same time, different from 2<sup>K</sup>, very close in value and mutually prime <sup>8,9</sup>.

In the search for moduli that would lead to logically "simple" modulo m adders, those of the form  $2^K$  +1 appear the most interesting ones after the lowcost  $^{3}$ ,  $^{4}$  moduli of the  $2^k$  -1 type and will be investigated here. For comparison with the better known  $2^k$  -1 modulus, the logic for this latter case will be derived anew, using the same type of approach that will be used for the  $2^k$  +1 case.

# 2. Two-level and one-level arithmetic for modulo m adders

Let x and y be two modulo m residues, coded in binary with k bits and let |x+y| denote the modulo m sum of x and y, i.e. the modulo m residue of the ordinary sum x+y. The network computing |x+y| will be called a (restricted) modulo m adder. Unrestricted adders might similarly be used as a name for adders that would accept any numbers x and y (not necessarily residues already) and compute |x+y| , but will not be considered here for the moment. Then we can write x, y and m (modulus) as pure binary integers.

$$x = o x_{k-1} ... x_{i} ... x_{o} m_{i}, x_{i}, y_{i} \in \{0,1\}$$

$$y = o y_{k-1} ... y_{i} ... y_{o} o \leq x, y < m$$

$$m = o m_{k-1} ... m_{i} ... m_{o} m_{k-1} = 1 (2^{k-1} \leq m < 2^{k})$$

where the assumption on m means that it is coded with k digits and no less. Then 14

$$|x+y|_{m} = x+y-v(t)m$$

$$t = \overline{sign}(x+y-m)$$
(2.2)

where v(u) is the arithmetic value of boolean u(1 for 1 and 0 for 0), sign X is the boolean sign 15.16 of X, equal to the leftmost, (k+1) the bit in 2's complement representation 15.16 (here sign x, sign y and sign m are zero, but have been explicitly represented in (2.1).

Equations (2.2) and (2.3) defined a two-level arithmetic procedure which is widely used in BCD arithmetic, iterative division networks 17 and in division algorithms based on the comparison method 14,15.16,22 . If left as such it can be implemented for instance with a sign detection network and an adder. If the sign detection function is a subfunction of a two-adder network computing first x+y-m, then +m may have to be restored by a third adder and this is analogous to the restoration method for a division step 14,15,22. In the following however we will derive explicit expressions for the subtract signal t. A first solution will be to use t as a gating signal to perform a conditional addition of the classical type. Another is to combine the logic of t with the adder logic to be subsequently used so as to obtain a scheme where sign-detection and adding step are fully intermeshed in what may how be called one level solution. Two level solutions for 2 k-1 moduli are well known for any k and one level solutions have been reperted for small specific values of k on and for arbitrary k (e.g. 13). Similarly two-level solutions are used in BCD arithmetic (moduli 5. and 10) and one level solutions, previously reported for small k's only 6, will be given for arbitrary k in this paper. Basic notations are defined in the appendix.

### 3. Sign-detection logic

For an arbitrary modulus m, subject to assumptions of  $\S.1$ , if we call  $r_i$  and  $r'_i$  the carries generated, respectively, in addition x+y and in subtraction (x+y)-m, then it can be shown 14 that

Sign 
$$(x+y-m) = maj(o, \overline{o}, r'_{k+1})$$
  
=  $r'_{k+1}$   
=  $maj(\overline{r_k}, o, r'_k)$   
=  $\overline{r_k}r'_{k+1}$  (3.0)

where  $r_k$  and  $r'_k$  can be expressed in turn as functions of  $x_i$ ,  $y_i$  and  $m_i$  variables to determine an explicit expression of t. Such computation will be presented below for moduli  $2^k$  -1 and  $2^k$  +1.

# 3.1 Sign-detection logic for modulus 2k -1

Let us write

$$S = x + y \tag{3.1}$$

Then

$$S = r_{k} s_{k-1} \dots s_{k}$$
 (3.2)

with (cf. appendix)

$$\begin{cases} s_{i} = x_{i} \oplus y_{i} \oplus r_{i} = P_{i} \oplus r_{i} & (r_{o} = 0) \\ r_{i+1} = G_{i}^{1} + P_{i} r_{i} \end{cases}$$
 (3.3)

Similarly, denote by S' the sum x+y-m and s'is digits

$$S' = S - m \tag{3.4}$$

$$S' = \dots s'_{k+1} s'_{k} \dots s'_{k} \dots s_{k}$$
 (3.5)

Then s'i and r'i are the sum and carry digits of a subtraction 15.16 given by

$$\begin{cases} S'_{i} = S_{i} \oplus m_{i} \oplus r'_{i} & (r'_{o} = 0) \\ r'_{i+1} = maj \left(\overline{S}_{i}, m_{i}, r'_{i}\right) \end{cases}$$
(3.6)

For modulus  $2^k$  --1, and for positions 0 to k-1inclusive

$$m_i = 1$$

and by recursively applying (3.6) or using an explicit carry expression 11,14,16,22 we get

$$r'_{k} = \sum_{j=0}^{k-1} \overline{S}_{j}$$

$$= \underbrace{\prod_{j=0}^{k-1} P}_{0k-1}$$

$$= \underbrace{\bigcap_{j=0}^{k-1} P}_{0k-1}$$
(3.7)

Whence

$$= T_{o,k-1} \tag{3.8}$$

This last term is the  $\frac{\text{transmitted carry}}{\text{tor block }[0,k-1]}$ , i.e. the value of output carry The block [0,k-,], i.e. the value of output carry  $r_0$  for an input carry  $r_0$  forced to 1. Usually in cyclic carry adders only the generated carry  $G_{0,k-1}$  (value of  $r_k$  for  $r_0$  forced to zero) is used. The result will remain equal to  $|x+y| \ge k - 1$  modulo  $2^k - 1$ , but, when x+y equals  $2^k - 1$ , will be left as such and will thus not be a residue.

### 3.2 Sign-detection logic for modulus 2k +1

Assume again x and y to be residues. They may require k+1 digits to be represented so that we will extend x, y and m representations one more position to the left and apply (3.0) for k+1 instead of k. Using the same symbols S, S', si, s'i, ri r'i for that new case, we have

$$\begin{cases} x = 0x_{k} x_{k-1} \dots x_{i} \dots x_{o} \\ y = 0y_{k} y_{k-1} \dots y_{i} \dots y_{o} \\ m = 01 \ 0 \ \dots 0 \dots 1 \end{cases}$$
 (5.9)

$$x+y = r_{k+1} s_k s_{k-1} ... s_{k-1} ... s_{k-1} (r_k carries)$$
(3.10)

$$x+y-m = ... s'_{k} s'_{k-1} ... s'_{k} ... s'_{k} ... s'_{k} ... s'_{k}$$
 (r' carries)

Then carries generated in positions 
$$[0,k-1]$$
 are decrementation carries 11;12.15 and  $r'_{k} = \prod_{j=0}^{k-1} \overline{s_{j}}$  (3.12)

$$r_{k+1}^{i} = maj(\bar{s}_{k}, 1, r_{k}^{i})$$
 (3.13)  
 $= \bar{s}_{k} + r_{k}^{i}$   
 $= \bar{s}_{k} + \prod_{j=0}^{m-1} \bar{s}_{j}$  (3.14)

$$=\overline{5}_{R}+\overline{1}_{1}\overline{5}_{3}$$

$$=3.14$$

Also

but if  $(x_k, y_k)$  equals one of the pairs (0,1) (1,0) (1,1) then carry  $r_k$  is zero as the first digits of x or y or both will be zero. Thus

$$\begin{array}{c}
f_{k} = 0 \\
f_{k+1} = G_{k} \\
\text{Finally}
\end{array}$$

sign 
$$[x+y-(2^{\frac{1}{k}}+1)] = \overline{r_{k+1}} r_{k+1}'$$
  
=  $\overline{G_k} (\overline{S_k} + r_k')$  (3.15)

$$t = G_{k} + S_{k} r_{k}^{-1}$$
 (3.16)

Note: If x and y are not constrained to be residues, then  $G_{0,k}$ , and not  $G_k$  should be used in (3.16).

### 4. Signed-carry adders for modulo 2k +1 arithmetic

Three solutions will be described corresponding to increasing integration of the subtract signal t with the adder logic. The least integrated scheme is an ordinary word-length adder with an iterative correction network on its output. In the second solution, ordinary full adder stages are still apparent (although not a word-length adder) and are supplemented with a correction network feeding signals between stages. In the last and most integrated design, a completely specialized ad der is evidenced, with a bidirectional iterative structure.

# 4.1 Adder with output correction network

In this scheme the ordinary addition is performed by a k position adder. A correction network is applied to outputs  $s_i$  ( $o \le i \le R$ ), computes t according to (3.16) and, using t as a gating signal, conditionally subtracts 2k +1. The latter operation is itself a decrement operation for positions 0 to k-1 inclusive and a special-purpose logic for rank k. Thus S' = x + y - v(t)

$$S' = x + y - v(t) \tag{4.1}$$

$$S'_{i} = S_{i} \oplus tr'_{i} \qquad (0 \le i \le k-1) \tag{4.2}$$

$$S'_{R} = S_{R} \oplus t \oplus t r'_{R}$$

$$= S_{R} \oplus t \overline{r'_{R}}$$

$$= (4.3)$$

$$\begin{aligned}
&= s_{k} \oplus t \overline{r_{k}'} \\
&t r_{i}' = \left[G_{k} + s_{k} \left(\sum_{j=0}^{k-1} s_{i}\right)\right] \left(\prod_{j=0}^{i-1} \overline{s_{j}}\right) \\
&= \left[G_{k} + s_{k} \left(\sum_{j=i}^{k-1} s_{j}\right)\right] \left(\prod_{j=0}^{i-1} \overline{s_{j}}\right) \\
&= \left(G_{k} + s_{k} S_{j}\right) S_{i}' \left(S_{i} = \sum_{j=i}^{k-1} s_{j} S_{j}' = \prod_{j=0}^{i-1} \overline{s_{j}}\right)
\end{aligned}$$

Terms  $S_i$  and  $S_i$  can be computed recursively from the left and the right respectively (Fig. 1 (a) cells) and combined with  $G_k$ ,  $s_k$  and  $s_i$  terms (Fig. 1(b) and (c) cells) according to (4.3,4.4).

#### 4.2 Adder with integrated sign-detection and add logic

Both adders in this category use the operation

$$x+y-v(u) \qquad u \in \{0,1\} \qquad (4.5)$$

If we have an operator to implement it, then it can be used for the k positions from the right, the k+1 th again being obtained by an ad hoc scheme. This will be obtained by using for u the function t. The procedure here parallels the one used for modulo  $2^k$  -1 addition where we perform

$$S' = x + y + v(t) \tag{4.6}$$

However, due to the fact that v (t)has now to be subtracted from x+y rather than added, another logic operator is needed which we will call signed carry adder, owing to the property it will eviden-

### 5. Signed-carry adders

#### 5.1 Definition

By definition such an adder will compute the

$$z = x + y + v(t'_c)$$
  $t'_o \in \{0, 1, \overline{1}\}$  (5.1)

The terminology and the choice of the domain for t'o may be justified as follows: if we try to add, digit by digit, the numbers x, y and -1, the partial sum for position 0 will be in the set  $\{-1,0,1,2\}$  and, if we code it in two's complement form, this will produce a carry in the set  $\{-1,0,1\}$  . Then for the next position the sum of the two digits and this carry will be in the

set  $\{-1,0,1,2,3\}$  which will again yield a carry in the set  $\{-1,0,1\}$ . So that, as soon as we assume t'o capable of taking the value  $\{-1,-1\}$ , all interstage carries will have a sign and no complication results from assuming to in the set { 1,0,1} (instead of 7,0 only).

# 5.2 Signed-carry adder stage logic

Let us call in general t; the signed carry into position i. We can write  $t'_{i} = (-1)^{v(t''_{i})} v(t_{i})$ 

$$t'_{i} = (-1)^{r(t''_{i})} r(t_{i}) \qquad t'_{i}, t''_{i} \in \{o, 1\}$$
 (5.2)

$$\zeta_{i}^{\prime} = -2^{1} v(t_{i}^{"} t_{i}) + 2^{\circ} v(t_{i})$$
 (5.3)

$$=-2^{2}v(t_{i}''t_{i})+2^{4}v(t_{i}''t_{i})+2^{9}v(t_{i})$$

The absolute value is  $v(t_1)$  and the usual sign is  $v(t_1^*)$  while the Boolean sign is  $t_1^*$  is  $t_1^*$  . Then we must have for every rank i:

$$V(x_i) + V(y_i) + t_i' = 2^1 V(t_{i+1}') + 2^{\circ} V(s_i)$$
 (5.4)

where s, will be the sum digit and to the new carry. This is an equation between two numbers, of which the binary digits must then be equal.

Each side can be calculated with binary addition rules . Denoting by ri the carries for that addition :

$$V(x_{i}) + V(y_{i}) + t'_{i} = -2^{2}V(s_{i}^{2}) + 2^{2}V(s_{i}^{2}) + 2^{2}V(s_{i}^{2})$$

$$S_{i}^{2} = x_{i} \oplus y_{i} \oplus t_{i} \qquad (5.5)$$

$$S_{i}^{1} = ma_{i}(x_{i}, y_{i}, t_{i}) \qquad r'_{2} = (x_{i} + y_{i})t''_{i}t_{i} \qquad (5.6)$$

$$T_{i}^{2} = (x_{i} + y_{i})t''_{i}t_{i}$$

$$s_{i}^{2} = \overline{z}_{i} \overline{y}_{i} t_{i}'' t_{i}$$

$$2^{1}v(t_{i+1}') + 2^{2}v(s_{i}) = -2^{2}v(t_{i+1}'' t_{i+1}) + 2^{1}v(t_{i+1}) + 2^{2}v(s_{i}')$$

Equating the two sides yields

$$\begin{cases} s_i = z_i \oplus y_i \oplus t_i \\ t_{i+1} = maj(z_i, y_i, t_i) \oplus t_i''t_i \\ t_{i+1}'' t_{i+1} = \overline{z}_i \overline{y}_i t_i''t_i \end{cases}$$
(5.8)

The last equation is of the form

$$ax = b$$

and is soluble if 19

$$[maj(x_i,y_i,t_i) \oplus \overline{t_i''t_i}][\bar{x}_i\bar{y}_i,t_i''t_i]=0$$

which can be seen to be identically true, so that

$$t_{i+1} = \overline{x_i} \overline{y_i} t_i'' t_i' + T(x_i, y_i, t_i'', t_i)$$
 (5.9)

where T is an arbitrary function of  $\mathbf{x}_i$  .  $\mathbf{y}_i$  ,  $\mathbf{t}_i^*$  and  $\mathbf{t}_i$  . It is possible to choose T so that, for instance

$$t_{i+1} = t_i'' t_i \tag{5.10}$$

Whatever the choice of T, the product ti ti meets the simple relationship (cf (5.8) and notations in appendix)

The logic for the signed-carry adder stage can be written in terms of zero generate  $(G_1^0)$  one generate  $(G_1^0)$ , 16,18 and propagate symbols  $(P_1)$  as follows:

$$S_i = P_i \oplus t_i$$
  $(0 \le i \le k-1)$  (5.12)

$$t_{i+1} = G_i' \oplus P_i t_i \oplus t_i'' t_i$$
 (5.13)

$$t_{i+1}^{"} = t_{i}^{"} t_{i} \qquad \left(t_{i+1}^{"} t_{i+1}^{'} = G^{\circ} t_{i}^{"} t_{i}^{"}\right) \qquad (5.14)$$

An iterative adder with cells implementing the above equations can be devised (Fig. 2). Each cell is slightly more complicated than an ordinary full-adder stage. But it is also possible to make use of ordinary adder stages, if we separately generate the  $t_1$ ,  $t_2$  products, to be used in the  $t_{i+1}$  relationship, by means of (5.13). We then get the scheme of Fig. 3. This is then very close in complexity to the scheme that would use an ordinary adder for x+y and a parallel decrementer 11,15 to subtract one. However the recursive computation with the (b) cells determines products of the G<sup>0</sup> terms (known before the adder starts computing) while in the solution with decrementer the product formed are of the si sum digits of the adder.

In general, the above computation is very close to the one that may be used for base -2 adders

# 5.3 Explicit carry logic for signed-carry adders

We can also express  $t_{i+1}$  as an explicit (non-recursive) function of variables  $G_{i}^{0}$ ,  $G_{i}^{1}$ .  $P_{i}$  in ranks 0 to i inclusive and of  $t_{i}^{0}$  and  $t_{i}^{0}$ . Let us denote by  $G_{0,i}$ ,  $P_{0,i}$  the ordinary generate and propagate functions for block 0,i-1 and by  $G_{0,i}^{0}$  the product of  $G_{i}^{0}$  terms (zero generate terms) from 0 to i-1 inclusive

$$G'_{o,i} = \prod_{i=0}^{i-1} G'_{i}$$
 (5.15)

$$t_{i+1} = G_i^1 \oplus P_i t_i \oplus G_{o,i-1}' t_o'' t_o$$
 (5.17)

We can now use this last formula to substitute  $\mathbf{t_{i}}$  , then  $\mathbf{t_{i-1}}$  etc. until all intermediate  $\mathbf{t_{i}^{\prime}}$  s have been eliminated. It can be seen that we

$$t_{i+1} = G_{o,i} \oplus P_{o,i} \circ \oplus G''_{o,i} \circ \circ$$
 (5.18)

$$G_{o,i} = G_i^1 + P_i G_{o,i-1}$$
 (5.19)

$$\overline{G_{o,i}} = G_i^o + P_i \overline{G_{o,i-1}}$$
 (5.20)

$$P_{o,i} = P_i P_{o,i-1}$$
 (5.21)

$$G_{0,i}'' = P_i G_{0,i-1}'' \oplus G_{0,i-1}'$$
 (5.22)

$$G'_{o,i} = G'_{i} G'_{o,i-1}$$
 (523)

where the first three are formulas 22 for the classical generate and propagate terms and the fourth one results from the elimination scheme.

Expression (5.18) is explicit and only uses three parameters  $G_{0,1}$ .  $P_{0,1}$  and  $G_{0,1}$  (versus  $G_{0,1}$  and  $P_{0,1}$  for classical adders) and the signed-carry of least significant weight. The  $G_{0,1}$  term can be simplified in (5.22). as

$$G''_{o,i}G'_{o,i} = \left[P_{i}G''_{o,i-1} \oplus G'_{o,i-1}\right]G'_{i}G'_{o,i-1}$$
 (5.24)

$$= G_{i}^{\circ} G_{o,i-1}'$$

$$= G_{o,i}'$$

$$\overline{G}_{o,i}' G_{o,i}' = 0$$
Hence, applying this to rank i-1
$$(5.25)$$

$$G''_{o,i} = (P_i \overline{G'_{o,i-1}}) \overline{G''_{o,i-1}} + \overline{P_i} G'_{o,i-1}$$
 (5.26)

which shows  $G_{0,i}^n$  to be of the form  $A+BG_{0,i-1}^n$  where A and B are separately computable. To build an explicit carry adder according to (5.18) it is sufficient to generate  $G_{0,1}$ ,  $P_{0,1}$  and  $G_{0,1}^{"}$  and combine the terms according to (5.18). Explicit expressions may be obtained for G", from repeated application of formulas (5.22) or (5.26) in much the same manner as for ordinary formulas (5.19,5.20) and yields terms of a similar complexity. For instance

$$G''_{0,3} = G''_{2}G''_{1}G''_{2} \oplus F_{3}G''_{2}G''_{2} \oplus F_{3}F_{2}G''_{2} \oplus F_{3}F_{2}F_{1}$$
 (5.27)

$$G'_{0,2} = G'_1 G'_0 \oplus P_2 G'_0 \oplus P_2 P_1$$
 $G''_{0,1} = G''_0 \oplus P_1$ 

Also, recursion formulas (5.15, 5.19, 5.21, 5.26) allow to build another adder, in which all carry magnitudes are function of the carry sign and magnitude in the rightmost position only  $(t_0'' t_0)$ . The logic is

$$5_{i} = P_{i} \oplus t_{i} \qquad (0 \leq i \leq k-1) \qquad (5.28)$$

$$t_{i+1} = G_{0,i} \oplus P_{0,i} t_0 \oplus G_{0,i}'' t_0'' t_0$$

with Go,1 , Po,1 , Go,1 and Go,1 generated recur-

#### 6. Iterative modulo 2k +1 adders

Modulo  $2^k$  +1 adders will have a regular structure for positions 0 to k-1 inclusive and a separate logic for position k. We will consider for the moment only the carry generation in block [0,k-1](which includes rk) and the sum generation in [0.k-1] and only later will consider the sum logic of the irregular stage k.

# 6.1 Adder with single decrement signal generation

Such an adder uses the signal t (3.16) according to (5.13) with:

$$\mathbf{t_0^n} \ \mathbf{t_0} = \mathbf{t} \tag{6.1}$$

The modulo  $2^k$  +1 adder thus uses, to generate the sum and carries in block [0,k-1] a signed-carry adder to which the subtract signal  $\bar{t}$  is fed as a least significant carry. It is convenient to take both  $t_0$  and  $t_0$  equal to t. In this solution , the main problem is to generate the signal t. As we do

not have a ordinary adder to provide the ordinary sums s; from which it could be computed, other logio must be used to obtain t in terms of what is now available as inputs, i.e. the  $G_1^0$  ,  $G_1^1$  ,  $P_1$ terms. Basically the difficult part is to obtain rk of which t is a simple function (3.16). Computation of rk

The term  $r_k$  , equal to the product of all  $\overline{s_j}$  is one if the result of ordinary addition, with  $r_0$ carry-in at the rightmost position, is all zeros, i.e. if the two numbers, limited to their first k positions, are either the boolean complement of each other  $(r_0 = 1)$ , or the true complement of each other  $(r_0 = 0)$ . The first situation happens if the addition block propagate  $P_0$  k-1 is one while the second happen if at some place in the two numbers, there is generation of 1, together with propagation on the left of it and generation of zero in all positions on the right. Thus we have a first way of expressing  $\mathbf{r_k}$  as an explicit function of all posi-

which may be used for short modules. For long modules however some recursion formula is necessary. To obtain one, consider the two conditions for a block of digits to produce an all-zero block of sum digits with respectively an input carry of 1 and an input carry of zero. For a block[/i,j] and a carry-in of 1, the function that signals that condition is the block propagation  $P_{i,j}$  . For the same block and a carry-in of 1, let us denote the allzero condition by  $R_{1,j}$  and also let us designate by  $Z_{1,j}$  the all-zero condition regardless of carry-in. Then we have

$$Z_{i,j} = R_{i,j} \overline{r_i} + P_{i,j} r_i$$
 (6.3)

where  $\mathbf{r}_{i}$  is the carry of ordinary addition. Then

$$r'_{k} = Z_{o,k-1}$$

$$= R_{o,k-1} \cdot (\bar{o}) + P_{o,k-1} \cdot (o)$$
(6.4)

$$= R_{o, k-1} \tag{65}$$

Now the  $R_{0,k-1}$  can be computed recursively, it turns out, either from the left or from the right of the words. For instance, from the left ("backward recursion") we have

$$R_{i,k-1} = R_{i+1,k-1}G_{i}^{\circ} + P_{i+1,k-1}G_{i}^{1}$$
 (6.6)

$$P_{i,k-1} = P_{i+1,k-1}P_{i}$$
 (6.7)

Once r; is generated,  $t_k$  itself is obtained thru (3.16 ) and may be then connected to the  $t_0$  , to or to to inputs of signed-carry adders of Fig. 2.3 and 4. The total propagation length is 2k positions (k positions in each direction), the same as if  $r_k$  were computed isolately by a forward recursion (6.18).

# 6.2 Adder with multiple decrement signal generation

The basic idea for this adder is to recompute separately for each variable position i the fixed term R<sub>0.k-1</sub> thru an expression adapted to each i. then to look for a recursive generation of such an expression, and finally, to combine it for possible simplification, with the Po, i terms which come into play for the same position For any position i, we have

$$Z_{o,k-1} = Z_{i+1,k-1}Z_{o,k}$$

$$= Z_{i+1,k-1}R_{o,i}$$

$$= (R_{i+1,k-1}\overline{r_{i+1}}) + P_{i+1,k-1}r_{i+1})R_{o,i}$$

$$= (R_{i+1,k-1}\overline{G_{o,i}} + P_{i+1,k-1}G_{o,i})R_{o,i}$$
(6.8)

an expression which as such would require the generation of the R terms both forward and backward. This is a possible scheme (in combination with (5.28)), for  $R_{0}$ , can also be obtained recursively as we will see below (6.18). However, another solution which we now consider is to determine the recursive parameters which will actually be needed after t is multiplied out by  $P_{0,i}$  and  $G_{0,i}^{"}$ . Thus

$$t_{o,i} = (G_{R} + s_{R} \overline{r_{R}^{\prime}}) P_{o,i}$$
 (6.10)

$$\frac{\mathsf{t} \, \mathsf{P}_{o,i}}{\mathsf{r}_{k}^{\prime} \, \mathsf{P}_{o,i}} = \left(\mathsf{G}_{k} + \mathsf{s}_{k} \, \overline{\mathsf{r}_{k}^{\prime}}\right) \mathsf{P}_{o,i} \qquad (6.10)$$

$$\frac{\mathsf{r}_{k}^{\prime} \, \mathsf{P}_{o,i}}{\mathsf{r}_{k}^{\prime} \, \mathsf{P}_{o,i}} = \left(\overline{\mathsf{R}_{i+1,k-1}^{\prime} \, \mathsf{G}_{o,i}} + \overline{\mathsf{P}_{i+1,k-1}^{\prime} \, \mathsf{G}_{o,i}} + \overline{\mathsf{R}_{o,i}^{\prime}}\right) \mathsf{P}_{o,i} \qquad (6.11)$$

$$= \overline{R_{i+1,k-1}} P_{i,i} + \overline{R_{o,i}} P_{o,i}$$
(6.12)

Now, for G"

$$\overline{r_{k}'G_{o,i}''} = \overline{R_{i+1,k-1}G_{o,i}G_{o,i}'' + P_{i+1,k-1}G_{o,i}G_{o,i}'' + R_{o,i}G_{o,i}''}$$
(6.13)

The five compound "forward" parameters Po,i

R<sub>0,i</sub> P<sub>0,i</sub>, G<sub>0,i</sub> G<sub>0,i</sub> G<sub>0,i</sub> G<sub>0,i</sub> and R<sub>0,i</sub>  $G_{0,i}^{"}$  could be computed from  $P_{0,i}$ ,  $G_{0,i}$ ,  $G_{0,i}^{"}$  and the first three of which are computable recursively as we saw before, while the fourth one will be found of that type also. Thus, we can set up two backward recursion chains and four forward chains and in each point 1 combine their values according to (6.6.6.7), and (5.15,5.19,5.21,5.26). The maximum propagation length for any i will be a constant number k of positions.

A last type of solution may be obtained by showing that the five above parameters are themselves computable thru recursions which are of the same type as for the four "primitive" parameters of which they are functions.

# 6.3 Recursion relationships for compound parameters

$$G_{o,i}''.G_{o,i} = \left(P_{i}G_{o,i-1}'G_{o,i-1}'' + P_{i}G_{o,i-1}'\right)\left(G_{i}^{1} + P_{i}G_{o,i-1}\right)$$

$$= P_{i}G_{o,i-1}'\left[G_{o,i-1}''G_{o,i-1}G_{o,i-1}\right] + G_{i}^{1}G_{o,i-1}'$$
(6.15)

$$G_{o,i}'' \overline{G_{o,i-1}} = \left( P_i \overline{G_{o,i-1}'} G_{o,i-1}'' + \overline{P_i} G_{o,i-1}' \right) \left( G_i' + P_i G_{o,i-1} \right)$$

$$= P_i \overline{G_{o,i-1}'} \left[ G_{o,i-1}'' \overline{G_{o,i-1}'} \right] + G_{o,i-1}'' G_{o,i-1}''$$
(6.16)

$$R_{o,i} = \left( R_{i,i} \overline{r_i} + P_{i,i} r_i \right) R_{o,i-1}$$
 (6.18)

$$R_{o,i} = \left(\overline{P_i} \overline{r_i} + P_i r_i\right) R_{o,i-1}$$

$$= \left(\overline{P_i} \overline{G_{o,i-1}} + P_i G_{o,i-1}\right) R_{o,i-1}$$

$$\overline{R_{o,i}} = \left(\overline{P_i} G_{o,i-1} + P_i \overline{G_{o,i-1}}\right) + \overline{R_{o,i-1}}$$

$$= \overline{P_i} \left(G_{o,i-1} + \overline{R_{o,i-1}}\right) + P_i \left(\overline{G_{o,i-1}} + \overline{R_{o,i-1}}\right)$$

$$(6.19)$$

$$G''_{o,i}\overline{R}_{o,i} = \overline{P_{i}}G'_{o,i-1}(G_{o,i-1} + \overline{R}_{o,i-1})$$

$$+ P_{i}\overline{G'_{o,i-1}}G''_{o,i-1}(\overline{G}_{o,i-1} + \overline{R}_{o,i-1})$$

$$= P_{i}G'_{o,i-1}[G''_{o,i-1}\overline{R}_{o,i-1}]$$

$$+ \overline{P_{i}}G'_{o,i-1}\overline{R}_{o,i-1} + P_{i}\overline{G'_{o,i-1}}G'_{o,i-1}\overline{G}_{o,i-1}$$

For the last identity we have used the fact that

$$G_{0,i} G_{0,i} = 0$$
 (6.21)

Also, it introduces two new compound parameters of the types  $G_{0,i}^{i}$   $\overline{R}_{0,i}^{0}$  and  $\overline{G}_{0,i}^{i}$   $G_{0,i}^{n}$   $\overline{G}_{0,i}^{0}$  which

themselves can be obtained thru recursions of the previous types. The first one is constantly zero and can be eliminated. The second is identical to the  $P_{0,i}$  parameter already generated:

$$G'_{o,i} \overline{R_{o,i}} = \left[ \overline{P_i} \left( G_{o,i-1} + \overline{R_{o,i-1}} \right) + \overline{P_i} \left( \overline{G_{o,i-1}} + \overline{R_{o,i-1}} \right) \right] G'_{o,i-1}$$
(6.22)

$$= G_{i}^{\circ} \left[ G'_{o,i-1} \overline{R_{o,i-1}} \right]$$

$$= G_{i}^{\circ} ... G_{i}^{\circ} G_{o}^{\circ} P_{o} = o$$

$$= G_{i}^{\circ} ... G_{i}^{\circ} G_{o}^{\circ} P_{o} = o$$

$$= G_{i}^{\circ} ... G_{i}^{\circ} G_{o,i-1}^{\circ} \left[ F_{i} G'_{o,i-1} \left( G'_{o,i-1} \overline{G'_{o,i-1}} \right) + G_{i}^{\circ} G'_{o,i-1} \right]$$

$$= P_{i} \left[ \overline{G'_{o,i-1}} G''_{o,i-1} \overline{G'_{o,i-1}} \right]$$

$$= P_{i} ... P_{i} \overline{G_{o}^{\circ}} \overline{1} \overline{G^{i}}$$

$$= P_{i} ... P_{i} P_{o} = P_{o,i}$$

$$= P_{o} ... P_{o} P_{o} = P_{o} P_{o}$$

Hence
$$G''_{o,i} \overline{R_{o,i}} = P_i \overline{G'_{o,i-1}} \left[ G''_{o,i-1} \overline{R_{o,i-1}} \right] + P_i P_{o,i-1}$$
Lastly
$$(6.24)$$

wich entails

$$\overline{r_k^2} \stackrel{\triangleright}{\rho_{i,i}} = \stackrel{\triangleright}{\rho_{i,i}} \tag{6.26}$$

$$t_{o,i}^{P} = (G_{g} + s_{g})_{o,i}^{P} \tag{6.27}$$

Thus  $t_{i+1}$ , for any i, can be generated with the six forward parameters  $G_{0,i}$ ,  $P_{0,i}$ ,  $G_{0,i}^{"}$ ,  $G_{0,i}^{"}$ ,  $G_{0,i}^{"}$ ,  $G_{0,i}^{"}$ ,  $G_{0,i}^{"}$ , which may be used instead of the five parameters  $G_{0,i}$ ,  $P_{0,i}$ ,  $G_{0,i}^{"}$ ,  $G_{0,i}^{"}$ ,  $P_{0,i}$ ,

Also in both solutions the backward parameters  $R_{i+1,k-1}$  and  $P_{i+1,k-1}$  are needed. With the six forward parameters solution, the cost of having an additional recursion chain should be weighed against the fact that  $\frac{1}{r_i}$   $G_{0,i}^n$  may be then generated, for each rank i, with 3 gates having 2, 2 and 3 inputs instead of 4 gates having 2,3,3,3 inputs. A design with the six parameter solution is given in Fig. 6. cells (a,b.c,c'.c") correspond to equations (6.6,6.7,6.14.6.16,6.20,6.24).

#### Initial conditions

$$G_{0,0} = G_0^1 \quad ; \quad G_{0,-1} = 0$$

$$P_{0,0} = P_0 \quad ; \quad P_{0,-1} = 1$$

$$G'_{0,0} = G_0^0 \quad ; \quad G'_{0,-1} = 1$$

$$R_{0,0} = \overline{P} \quad ; \quad R_{0,-1} = 1$$

$$G''_{0,0} = 1 \quad ; \quad G''_{0,-1} = 0$$

$$G''_{0,0}G_{0,0} = G_0^1 \quad ; \quad G''_{0,-1}G_{0,-1} = 0$$

$$G''_{0,0}\overline{G_{0,0}} = G_0^1 \quad ; \quad G''_{0,-1}G_{0,-1} = 0$$

$$G''_{0,0}\overline{G_{0,0}} = P_0 \quad ; \quad G''_{0,-1}\overline{G_{0,-1}} = 0$$

$$R_{0,0}R_{0,0} = P_0 \quad ; \quad G''_{0,-1}R_{0,-1} = 0$$

$$R_{0,0}R_{0,0} = P_0 \quad ; \quad G''_{0,-1}R_{0,-1} = 0$$

$$R_{0,0}R_{0,0} = P_0 \quad ; \quad G''_{0,-1}R_{0,-1} = 0$$

$$R_{0,0}R_{0,0} = P_0 \quad ; \quad G''_{0,-1}R_{0,-1} = 0$$

$$R_{0,0}R_{0,0} = P_0 \quad ; \quad G''_{0,-1}R_{0,-1} = 0$$

$$R_{0,0}R_{0,0} = P_0 \quad ; \quad G''_{0,-1}R_{0,-1} = 0$$

In rank k we must add the signed carry for signed-carry addition x+y-v (t) and also subtract v(t) (corresponding to the  $2^k$  component of modulus  $2^k+1$ ). The sign  $t^n_i$  of the incoming carry into position k will not appear in the expression of the sum digit and we will have

$$S_{\mathbf{k}}^{*} = (P_{\mathbf{k}} \oplus L_{\mathbf{k}}) \oplus L$$

$$= S_{\mathbf{k}} \oplus L$$

$$(6.28)$$

where  $s_k$  is the sum resulting from the use of  $t_k$  in the same way as for positions 0 to k-1 and t is  $G_k + s_k = \frac{R_{0,k-1}}{R_{0,k-1}}$ , in which all three terms are also

generated from the network. Thus the above network is irregular for position k.

### 7. Alternate designs

We may wish to fuse the  $s_k$  term, in the expression of t, with the logic expressions of  $\overline{\mathbf{r}_{k}^{t}}$  , so as to leave only the variables at rank k ( $G_k$ ,  $s_k$ or  $T_k$ ) as the irregular terms. As we have seen (3.16)

$$t = r_{k+1} + s_k r_k^{r_r}$$

$$r_{k+1} = G_{o,k}$$
(7.1)

$$=G_{k} + T_{k}G_{0,k-1}$$
 (7.2)

$$s_{k} = P_{k} \oplus r_{k}$$
 (7.3)

$$= P_{k} \oplus G_{0,k-1} \tag{7.4}$$

$$= \overline{G}_{k} T_{k} \oplus G_{0,k-1}$$
 (7.5)

Then

$$\begin{aligned}
t &= (G_{k} + T_{k} G_{0,k-1}) + (\overline{G_{k}} T_{k} \oplus G_{0,k-1}) \overline{r_{k}'} & (7.6) \\
&= \overline{G_{k}} T_{k} G_{0,k-1} \overline{r_{k}'} + \overline{G_{k}} T_{k} (G_{0,k-1} + \overline{G_{0,k-1}} T_{k}') + G_{k} T_{k} \\
&= G_{k} + T_{k} G_{0,k-1} \overline{r_{k}'} + T_{k} (G_{0,k-1} + \overline{r_{k}'}) & (7.7)
\end{aligned}$$

$$\begin{aligned}
tP_{0,i} &= G_{R_{0,i}} + T_{R_{0,i}} G_{0,k-1}P_{0,i} + T_{R_{0,i}}P_{0,i} \\
&= (G_{R_{0,i}} + T_{R_{0,k-1}} + T_{R_{0,i}})P_{0,i} \\
&= (G_{R_{0,i}} + T_{R_{0,k-1}})P_{0,i} \\
&= (T_{R_{0,i}} + G_{0,k-1})P_{0,i} \\
&= (T_{R_{0,i}} + G_{0,k-1})P_{0,i} \\
&= (T_{R_{0,i}} + G_{0,k-1})P_{0,i}
\end{aligned} \tag{7.8}$$

$$= ( {}^{\prime}_{k} + {}^{\prime}_{G_{i+1}, k-1} ) {}^{\prime}_{o,i}$$

$$t G_{o,i}^{"} = G_{k} G_{i}^{"} + T_{k} G_{o,k-1} K_{o,i} + T_{k} (G_{o,k-1} G_{i}^{"} + \frac{r_{i}^{\prime}}{k} G_{o,i}^{"} )$$

$$(7.9)$$

with
$$G_{0,k-1}P_{k}G_{0,i}'' = (G_{i+1,k-1} + P_{i+1,k-1}G_{0,i}) + P_{i+1,k-1}G_{0,i} + P_{0,i})G_{0,i}'$$

$$= G_{i+1,k-1}\overline{R_{i+1,k-1}} + G_{i+1,k-1}G_{0,i} + P_{0,i}G_{0,i}G_{0,i}''$$

$$+ G_{i+1,k-1}\overline{R_{0,i}} + P_{i+1,k-1}G_{0,i}F_{0,i}G_{0,i}G_{0,i}''$$

$$+ G_{i+1,k-1}\overline{G_{0,i}} + P_{k+1,k-1}G_{0,i}F_{0,i}G_$$

$$+ G_{i+1,k-1} G_{o,i} + G_{i+1,k-1} \overline{R_{o,i}} + P_{i+1,k-1} G_{o,i} + P_{i+1,k-1} G_{o,i} + G_{i+1,k-1} G_{o,i} + G_{i+1,k-1} \overline{R_{o,i}} + P_{i+1,k-1} G_{o,i} \overline{R_{o,i}} + T_{k} G_{i+1,k-1} \overline{R_{o,i}} G_{o,i} G_{o,i}$$

$$(7.15)$$

Thus the carry  $t_{i+1}$  (cf (5.18) ) can be computed from  $G_{0,i}$ ,  $tP_{0,i}$  and  $tG_{0,i}$  obtained above. With expressions (7.9.7.14) it can be implemented with forward parameters  $G_{0,i}$ ,  $P_{0,i}$ ,  $G_{0,i}^G$ ,  $G_{0,i}^G$ ,  $G_{0,i}^G$ ,  $G_{0,i}^G$ 

(or  $G_{0,i}$ ,  $P_{0,i}$  ,  $G_{0,i}$  ,  $G_{0,i}$  ,  $\overline{R_{0,i}}$  ,  $\overline{R_{0,i}}$  ,  $G_{0,i}$   $G_{0,i}$  and  $G_{0,i}^{n}$  which again involves one more chain, but simpler gates). The generation of  $G_{0,i}^{n}$  may be then

avoided if T may be assumed zero. This would be the case if  $\ ^k$  we treated separately the case where one or both operands equal  $2^k$  and the other cases. Such a scheme would involve a  $T_k$  gate, to switch the computation to either one of two networks, one to form a number equal to  $v(G_k)$   $(2^k-1)$  if  $T_k$  is

one and to use the above network for  $T_{\mathbf{k}}$  = 0. Then this operating constraint, the above network would simplify to

$$C_{i+1} = G_{o,i} \oplus P_{o,i} t \oplus G_{o,i}'' t \tag{7.16}$$

$$P_{0,i}t = G_{i+1,k-1}P_{0,i}$$
 (7.17)

$$G''_{o,i} = G_{i+1, k-1} \overline{R_{i+1, k-1}} + G_{i+1, k-1} G_{o,i} + G_{o,i}$$

dues, but this is not necessary for the more general one described by (7.9.7.14).

Both types of networks in §.7 require a backward recursion to generate the Gi,k terms. This can be done with the relationship 13.

$$G_{i,k} = G_{i+1,k} + P_{i+1,k} G_{i}$$
Appendix
$$(7.19)$$

In ordinary addition of binary numbers x and y the generate, propagate and transmit functions are defined as follows. For a block [0,i] of digits and an adder assumed to operate on the digits xj, yj for this block ( $0 \le j < i$ ), then the generate function is the carry out of position i, for a carry into position 0 equal to zero and the transmit function is the carry out of the same position when the carry into position 0 is a one. The propagate function for block [0,1] is the product of propagate functions for each position j. Let us use + for the logical sum (inclusive OR), 
for the exclusive OR, concatenation for the product (AND) of variables and overbars for complements. Let us denote for any block[i,j] (i  $\leq$  j) of digits  $G_{i,j}$ ,  $\mathbf{r}_{i,j}$  and  $\mathbf{r}_{i,j}$  the generate, transmit and propagate functions. Then we have the following relationships and conventions 15,16,18,21 :

(i) properties:

$$P_{0,i} = \int_{j=0}^{i} P_{j}$$

$$P_{j} = z_{j} \oplus y_{j}$$

$$G_{0,i} = G_{i}^{1} + P_{i} G_{0,i-1} ; G_{i}^{1} = z_{i} y_{i}$$

$$G_{0,i} = G_{0}^{0} + P_{i} G_{0,i-1} ; G_{i}^{0} = \overline{z}_{i} \overline{y}_{i}$$

$$T_{0,i} = G_{0,i} + P_{0,i}$$

$$G_{0,i} = G_{j+1,i} + P_{j+1,i} G_{0,j}$$

(ii)conventions:

$$G_{i,i} = G_i$$
 ;  $G_{i,i-1} = 0$   
 $P_{i,i} = P_i$  ;  $P_{i,i-1} = 1$   
 $T_{i,i} = T_i$  ;  $T_{i,i-1} = 1$ 

 $G_{i}^{1}$  and  $G_{i}^{0}$  are so-called 0-generate and 1-generate terms respectively.

#### References

- H.L. Gardner, "Error Codes for Arithmetic Operations," <u>IEEE Trans. Elect. Computers</u>, vol. EC-15, pp. 763-770, Oct. 1966.
- W.W. Peterson, <u>Error Correcting Codes</u>, MIT Press Cambridge, 1965.
- A. Avižienis, "Arithmetic Algorithms for Error coded Operands," 1972 Intern. Fault-tolerant Computing Symposium, Papers, pp. 25-34, June 1972.
- 4. A. Avižienis, "Arithmetic Error Codes: Cost and Effectiveness Studies for Application in Digital System Design," <u>IEEE Trans. on Computers</u>, Vol. C-20, N° 11, pp. 1321-1331, Nov. 1971.
- T.R.N. Rao, "Error-Checking Logic for Arithmetic-type Operations of a Processor, <u>IEEE Trans.on Computers</u>, Vol. C-17, pp. 845-849, Sept. 1968.
- A.E. Pertmann, <u>Circuits for Checking Arithmetic</u> <u>Errors by Means of Residue Coding</u>, AD 687095, <u>Feb. 1969</u>.
- 7. A. Svoboda, "Le Système Numérique des Classes Résiduelles Dans les Machines Mathématiques," Automatisme, Vol. 5, Nos 1 and 2,pp. 16-24, pp. 65-69, 1960.
- N.S. Szabo, R.I. Tanaka, <u>Residue Arithmetic</u> and its <u>Application to Computer Technology</u>, <u>McGraw Hill</u>, New York, 1967.
- T.R.N. Rao, O.N. Garcia, "Cyclic and Multiresidue Codes for Arithmetic Operations," <u>IEEE</u> Trans. Inform. Theory, Vol. IT-17, pp. 85-91, Jan. 1971.
- A. Avižienis, "Digital Computer Arithmetic: a Unified Algorithmic Specification," Symposium on Computers and Automata, Pol. Inst. of Brooklyn (13-15 April 1971) Papers. pp. 509 525.

- R.K. Richards, <u>Digital Design</u>, Wiley, New York 1971.
- 12. N.R. Scott, Electronic Computer Technology, McGraw Hill, New York, 1970.
- 13. J.P. Chinal, Single-Zero Digit Complement
  Adders, UCLA Comp. Science Department, Internal Memorandum, Nov. 1974. (in press)
- 14. J.P. Chinal, Détection et Correction Synchrones d'Erreurs Arithmétiques dans les Processeurs, ENSAE, Toulouse, 100p, March 1973.
- J.P. Chinal. <u>Microsystèmes Numériques</u>. ENSAE. Toulouse, 270 p. Jan. 1972.
- J.P. Chinal, Théorie Microanalytique des Processeurs Arithmétiques, ENSAE, Toulouse, 90 p. June 1973.
- 17. K.J. Dean, "Logical Circuits for Use in Iterative Arrays," <u>Electronic Letters</u>, 4, pp. 81-82, March 1968.
- M. Carvallo, <u>Principes et Applications de l'A-nalyse Booléenne</u>, Gauthiers-Villars, Paris 1965.
- 19. J.P. Chinal, <u>Boolean Features of Base-2 Signed Carry Adders</u>, UCLA, Computer Science Dept.Note, (in press)
- 20. G.C. Langdon, C.K. Tang, "Concurrent Error Detection for Group Look-Ahead Binary Adders,"

  IBM Journal of Res. and Development. , pp. 563-573, Sept. 1970.
- I. Flores, <u>The Logic of Computer Arithmetic</u>, Prentice Hall. 1963.

#### ACKNOWLEDGMENTS

This work was done while the author was with UCLA Computer Science Department as a US-France exchange scientist. The support of National Science Foundation, Washington. and of ENSAE, Toulouse, is gratefully acknowledged.

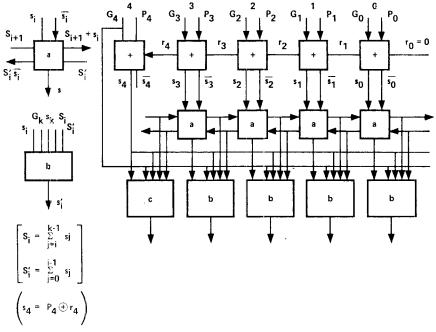


Figure 1. Classical Adder with Output Correction Network for Moduls  $2^k+1$  Addition. (k=4)

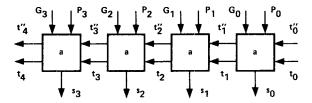


Figure 2. Signed-Carry Adder.

Logic:  

$$\begin{aligned} s_i &= P_i \oplus t_i ; t_{i+1} = G_i \oplus P_i t_i \oplus t_i'' t_i ; t_{i+1}'' = t''_i t_i \\ \end{aligned}$$
Arjthmetic Value of Carry:  

$$t_i' &= (-1)^{v(t_i'')} v(t_i)$$

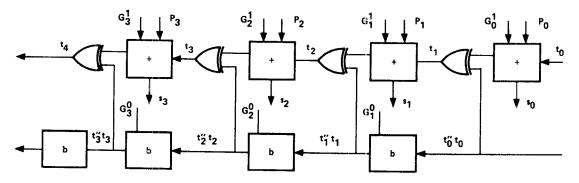


Figure 3. Signed-Carry Adder with Ordinary Adder Stages.

(+) cell: ordinary full adder

(b) cell: and gates

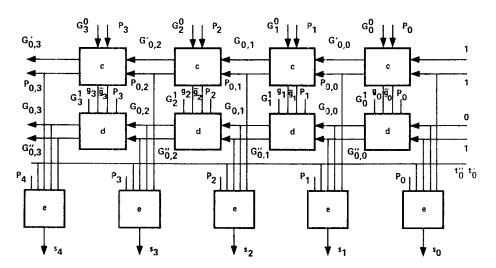
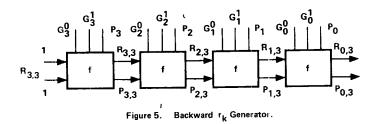


Figure 4. Signed Carry Adder with  $G_{0,i}$ ,  $G_{0,i}^{\prime}$ ,  $G_{0,i}^{\prime}$ ,  $P_{0,i}$  Interstage Variables,  $(g_i = G_{0,i-1}^{\prime})$ 



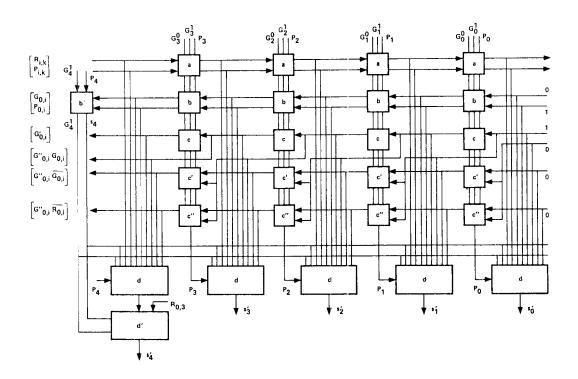


Figure 6. Another Modulo 2<sup>k</sup>+1 Adder with Six Forward Chains and Two Backward Chains.