

CONTENTS

SESSION I

Chairman: R. T. Gregory

- 1.1 *Basic Digit Sets for Radix Representation of the Integers*
D. W. Matula 1
- 1.2 *Exact Arithmetic Using a Variable-Length p -adic Representation*
R. N. Horspool and E. C. R. Hehner 10
- 1.3 *An Interleaved Rational/Radix Arithmetic System for High-Precision Computations*
K. Hwang and T. P. Chang 15

SESSION 2

Chairman: W. J. Cody

- 2.1 *A Unified Approach to a Class of Number Systems*
I. Koren and Y. Maliniak 25
- 2.2 *A Feasibility Analysis of Binary Fixed-Slash and Floating-Slash Number Systems*
D. W. Matula and P. Kornerup 29
- 2.3 *A Feasibility Analysis of Fixed-Slash Rational Arithmetic*
P. Kornerup and D. W. Matula 39
- 2.4 *A Modified Bi-Imaginary Number System*
A. G. Slekyš and A. Avižienis 48

SESSION 3

Chairman: D. W. Matula

- 3.1 *Required Scientific Floating Point Arithmetic*
L. A. Liddiard 56
- 3.2 *Desirable Floating-Point Arithmetic and Elementary Functions for Numerical Computation*
T. E. Hull 63
- 3.3 *A Realistic Model for Error Estimates in the Evaluation of Elementary Functions*
K. S. Frankowski 70
- 3.4 *Some Experiments Using Interval Arithmetic*
E. K. Reuter, J. P. Jeter, J. W. Anderson and
B. D. Shriver 75

SESSION 4

Chairman: P. Kornerup

4.1	<i>Multivariable Polynomial Processing - Applications to Interpolation</i> E. V. Krishnamurthy and H. Venkateswaran	81
4.2	<i>On Arithmetic Inter-relationships and Hardware Interchangeability of Negabinary and Binary Systems</i> D. P. Agrawal	88
4.3	<i>An Approximate and Empirical Study of the Distribution of Adder Inputs and Maximum Carry Length Propagation</i> O. N. Garcia, H. Glass, and S. C. Haines	97
4.4	<i>On Modular (2^n+1) Arithmetic Logic</i> D. P. Agrawal and T. R. N. Rao	104

SESSION 5

Chairman: T. C. Chen

5.1	<i>Logical Design of a Redundant Binary Adder</i> C. Y. Chow and J. E. Robertson	109
5.2	<i>Parallel Adders Using Standard PLAs</i> A. Weinberger	116
5.3	<i>A Comparison of Two Approaches to Multi-Operand Binary Addition</i> D. E. Atkins and S. C. Ong	125

SESSION 6

Chairman: J. E. Robertson

6.1	<i>Multiple Addition of Binary Serial Numbers</i> L. Dadda	140
6.2	<i>High-Speed Multiplication and Multiple Summand Addition</i> R. S. Lim	149
6.3	<i>The Theory and Implementation of High-Radix Division</i> D. G. Tan	154
6.4	<i>Higher Radix On-Line Division</i> K. S. Trivedi and J. G. Rusnak	164

SESSION 7

Chairman: L. Dadda

7.1 *Convergence Guarantee and Improvements for a Hardware Exponential and Logarithm Evaluation Scheme*
C. Wrathall and T. C. Chen 175

7.2 *An On-Line Square Rooting Algorithm*
M. D. Ercegovac 183

7.3 *An Arithmetic Module for Efficient Evaluation of Functions*
M. D. Ercegovac and M. M. Takata 190

7.4 *Two Methods for Fast Integer Binary-BCD Conversion*
F. A. Schreiber and R. Stefanelli 200

SESSION 8

Chairman: E. V. Krishnamurthy

8.1 *Arithmetic Circuit Fault Detection By Modular Encoding*
A. Svoboda 208

8.2 *Application of the Residue Number System to Computer Processing of Digital Signals*
G. A. Jullien and W. C. Miller 220

8.3 *Mathematical Approach to Iterative Computation Networks*
D. Cohen 226

8.4 *Merged Arithmetic for Signal Processing*
E. E. Swartzlander, Jr. 239

SESSION 9

Chairman: B. D. Shriver

9.1 *Design of Arithmetic Elements for Burroughs Scientific Processor*
D. D. Gajski and L.P. Rubinfeld 245

9.2 *Survey of Arithmetic Integrated Circuits*
S. Waser 257

9.3 *Computational Design Alternatives with Microprocessor-Based Systems*
S. L. Lillevik and P. D. Fisher 267

AUTHOR INDEX 274