A SYSTEMATIC APPROACH TO THE DESIGN OF STRUCTURES FOR ARITHMETIC

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A design tool for the decomposition of binary digital structures for addition and subtraction has been developed. A simplified theory reduces a complex structure to a collection of basic structures of one type, namely, a full adder. The simplified theory is applicable to the design of parallel counters and array multipliers. A general theory is used for decomposition to three types of basic structures, whose complexity is usually on the order of a half-adder. The general theory is applicable to redundant array multipliers and signed-digit adders.

1. Introduction

The purpose of this paper is to describe a theory of decomposition of complex structures for addition and subtraction. Some aspects of a simplified version of the theory are known, and will be used as an introduction. The necessary theoretical background will then be developed, and the general theory will be described. Applications of the theory to parallel counters, array multipliers, and signed-digit adders are given.

2. Design of a Parallel Counter with 7 Inputs

Consider first the design of a parallel counter whose inputs consist of seven binary digits of equal weight and whose outputs are three weighted binary digits, with weights 4, 2, and 1. The purpose of the parallel counter is to represent the number of input "ones" as a conventional binary number. The basic building block for a parallel counter is a binary full adder, which transforms three bits of equal weight into two bits, one of weight 2 and one of weight 1. The design of a 7 bit parallel counter is shown in Figure 1. In the figure

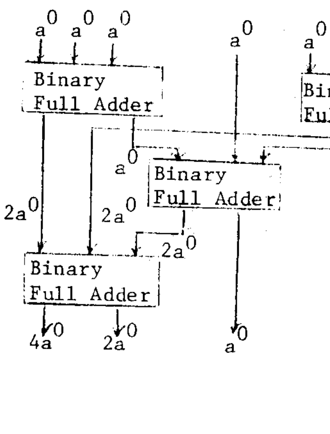

Fig. 1. Seven Bit Parallel Counter

the binary digit set {0,1} is represented by the notation a^0 ; a binary full adder is represented by the expression $2a^0+a^0 \leftarrow a^0+a^0+a^0$; and the 7-bit parallel counter in three levels, performs the operation

$$4a^0+2a^0+a^0 \leftarrow a^0+a^0+a^0+a^0+a^0+a^0+a^0$$

The input level of the structure consists of two binary full adders and performs the operation

$$(2a^0+a^0)+(2a^0+a^0)+a^0 \leftarrow (a^0+a^0+a^0)+(a^0+a^0+a^0)+a^0.$$

The intermediate level (one full adder) then performs

$$2a^0+2a^0+(2a^0+a^0) \leftarrow 2a^0+2a^0+(a^0+a^0+a^0)$$

The output level (one full adder) then performs

$$(4a^0+2a^0)+a^0 \leftarrow (2a^0+2a^0+2a^0)+a^0$$

These algebraic manipulations may be summarized by the information loss chart of Table 1.

λ	4	2	1
7			7
5		2	3
4		3	1
3	1	1	1

Table 1. Information Loss Chart For 7-Bit Parallel Counter

In Table 1, the left column (headed λ) indicates the information content, or total number of bits, for the corresponding row. The remaining columns indicate the number of bits of each weight (indicated by the heading) between successive levels of the structure. The change in the value of λ between successive rows indicates the number of full adders used at the corresponding level of the design of Figure 1. The total cost (in binary full adders) is $\lambda_{in}-\lambda_{out}$ = 7-3, or 4 full adders, and can be predicted from the original design specification. The information loss chart represents an abbreviated connectivity diagram, equivalent to the design of Figure 1.

3. Digit Sets

The function of a structure is to transform one or more input digit sets into one or more output

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digit sets in accordance with the rules of arithmetic. The properties of digit sets are as follows:

3.1 A (δ+1)- valued digit set is a sequence of $\delta+1$ consecutive integers $-\omega, -\omega+1\ldots, -\omega+\delta$.

3.2 A digit set is <u>normalized</u> if $\omega = 0$. It is convenient, and sometimes mandatory, to employ normalized digit sets in the initial phases of design.

3.3 A digit set is <u>symmetric</u> if δ is even and $\omega = \frac{\delta}{2}$. It follows that for any element x of a symmetric digit set, -x is also an element of the digit set. This property is particularly useful for subtraction.

3.4 The <u>diminished cardinality</u> δ of a digit set is one less than the number of values. The diminished cardinality is also the largest value in a normalized digit set.

3.5 A digit set is redundant if $\delta > r-1$, where r is the radix.

3.6 A composite digit set is a combination of two or more appropriately weighted digit sets. For example, an adder output σ is usually represented by a carry c and a sum s, with $\sigma = rc+s$. If the diminished cardinalities of the digit sets of σ, c and s are δ_σ, δ_c and δ_s respectively, then $\delta_\sigma = r\delta_c+\delta_s$. If all possible values of σ are to be consecutive integers, (and hence conform to the definition of a digit set) it is necessary that $\delta_s \geq r-1$.

3.7 The range of the diminished cardinality of a digit set is $1 \leq \delta \leq 2(r-1)$. The lower limit is essential; the upper limit is arbitrary, but sufficiently large for most practical purposes.

3.8 The magnitude of the smallest integer of a digit set is the <u>offset</u> ω of the digit set. A normalized digit set is converted to a generalized digit set by subtracting the offset ω from each value of the normalized digit set.

3.9 Zero is always an element of a digit set. This implies that the smallest value $-\omega$ satisfies $0 \leq \omega \leq \delta$.

3.10 The negative of a digit set is found by replacing each element of the digit set by its negative. As noted in 3.3, a symmetric digit set is its own negative. More generally if ω' is the offset of the negative of a digit set, then $\omega+\omega' = \delta$, where ω and δ are the offset and diminished cardinality of the original digit set.

3.11 Digit sets will be denoted by letters of the alphabet; the letter a for a digit set of diminished cardinality 1, b if $\delta = 2$, i if $\delta = 9$, etc. The offset is designated by a superscript, thus a^0 is the digit set {0,1}, a^1 is the digit set $\{\bar{1},0\}$, b^1 is the digit set $\{\bar{1},0,1\}$ and i^0 is the digit set {0,1,2, 3,4,5,6,7,8,9}.

4. <u>Elementary Structures</u>

The simplest of structures preserve certain essential relationships between input digit sets and output digit sets, in accordance with the basic rules of arithmetic. First, the weighted sum of the diminished cardinalities of the output digit sets is always equal to the sum of the diminished cardinalities of the input digit sets. For a binary full adder, $2a^0+a^0 = a^0+a^0+a^0$, where each digit set a^0 has a diminished cardinality of 1, the equation is 2+1 = 1+1+1. This property that a structure preserves diminished cardinality follows directly from the basic properties of addition and subtraction, and is easily proved in general. It is therefore possible, since the diminished cardinalities of a structure are the same at the input and at the output, to characterize a structure by its diminished cardinality.

Similarly, a basic structure preserves offset. If $z = x+y$ represents a structure for which z,x, and y are each elements of normalized digit sets, then, $(z-\zeta) = (x-\xi)+(y-\eta)$ also represents a structure, where $\zeta = \xi+\eta = \omega$, the offset. Thus, offset is also preserved, and it is proper to characterize a structure by its offset.

At this point, the elements of a classification scheme for structures become apparent; namely,

1) the radix r,
2) the diminished cardinality δ, and
3) the offset ω.

Under the classification $r.\delta.\omega$, the simplest of structures may now be listed, using the notation of 3.11, beginning with structures with offset 0.

2.2.0	$b^0 \leftarrow a^0+a^0$	Generalized half adder
	$a^0+a^0 \leftarrow b^0$	Converter
2.3.0	$2a^0+a^0 \leftarrow b^0+a^0$	Carry generator
	$b^0+a^0 \leftarrow 2a^0+a^0$	Inverse carry generator
	$2a^0+a^0 \leftarrow a^0+a^0+a^0$	Full adder
	$a^0+a^0+a^0 \leftarrow 2a^0+a^0$	Inverse full adder

Use of non-zero values of offset (i.e., digit sets which are not normalized) is indicated by use of a non-zero superscript, and introduces structures for subtraction. Examples are

2.2.1	$b^1 \leftarrow a^0+a^1$	Generalized half subtracter
2.3.2	$2a^1+a^0 \leftarrow a^1+a^1+a^0$	Full subtracter

An important result, due to Nguyen [12.11], is that the three structures, with their variants,

$b \leftarrow a+a$	Generalized half adder
$a+a \leftarrow b$	Converter
$2a+a \leftarrow b+a$	Carry generator

are sufficient for the realization of more complex structures for addition and subtraction. For example, the full adder $2a^0+a^0 \leftarrow a^0+a^0+a^0$ is a combination of the carry generator $2a^0+a^0 \leftarrow b^0+a^0$ and the generalized half adder $b^0 \leftarrow a^0+a^0$.

An important observation is that since the elementary structures preserve diminished cardinality, then more complex structures to be decomposed must also preserve diminished cardinality.

Three cases may occur.

1) $\delta_{out} < \delta_{in}$ The structure is not realizable since not all input values can be represented by the output.
2) $\delta_{out} = \delta_{in}$ The structure is realizable and decomposable.
3) $\delta_{out} > \delta_{in}$ The structure is realizable, but not decomposable. The structure may be made decomposable by the addition of mythical inputs, such that $\delta_{out} = \delta_{in}+\delta_{myth}$. The mythical inputs may later be used to simplify the design.

5. Design of a Parallel Counter with 5 Inputs

For this design, the output is $4a^0+2a^0+a^0$, with $\delta_{out} = 7$, as in section 2, but the input is $a^0+a^0+a^0+a^0+a^0$, with $\delta_{in} = 5$. It is therefore necessary to add an input $2a^0$ with $\delta_{myth} = 2$. The information loss chart becomes

	λ	4	2	1
Input	5			5
Mythical Input	1		1	
Decomposable Input	6		1	5
	5		2	3
	4		3	1
	3	1	1	1

Table 2. Information Loss Chart For 5 Bit Parallel Counter

For this design, three adders are necessary, except that the adder used to reduce λ from 4 to 3 has one input which is mythical, and hence always 0. Therefore, this adder may be replaced by a half adder, and the total cost is 2 full adders and one half adder.

6. Logical Design and Formats for Three-Valued Digit Sets

For purposes of logical design, it is necessary that the three valued digit set b*in all its variants $b^0 = \{0,1,2\}$, $b^1 = \{\bar{1},0,1\}$, and $b^2 = \{\bar{2},\bar{1},0\}$, be represented by two binary digits. For each variant, there are 72 ways this can be done, which can be reduced to 9 groups of eight, called formats, under permutation and negation of the two binary digits. For brevity, only two formats will be considered here, as indicated in Tables 3a, 3b, 4a, and 4b.

b^0	a^0	a^0	b^1	a^1	a^0
0	0	0	0	0	0
1	0	1	1	0	1
1	1	0	$\bar{1}$	$\bar{1}$	0
2	1	1	0	$\bar{1}$	1

Table 3. Format 1

*Absence of a superscript indicates the class of structures including all variants due to changes in offset values.

b^0	a^0	a^0	b^1	a^1	a^0
0	0	0	0	0	0
1	0	1	1	0	1
2	1	0	DC	$\bar{1}$	0
DC	1	1	$\bar{1}$	$\bar{1}$	1

Table 4. Format 2

The third variant, $b^2 \leftarrow a^1+a^1$, is simply the negative of $b^0 \leftarrow a^0+a^0$, in each case.

For format 1, the relations $b^0 \leftarrow a^0+a^0$ and $b^1 \leftarrow a^1+a^0$ hold, and therefore the converter and generalized half adder require no hardware whatsoever. The carry generator $2a+a \leftarrow b+a$ becomes a full adder $2a+a \leftarrow a+a+a$, and, in all its variants, is the only elementary structure necessary for decomposition. Format 1 is thus the basis for the examples of parallel counters given in sections 2 and 5.

For format 2, the generalized half-adder $b \leftarrow a+a$ becomes a half adder, and the carry generator $2a+a = b+a$ is a half adder with the extra OR gate needed to complete a full adder. The converter $a+a \leftarrow b$ is a single OR gate. The remaining formats, 3 through 9, are either too complicated to merit consideration, or tend to decrease the cost of the generalized half adder by one or two gates at the expense of a corresponding increase in the cost of the carry generator. Thus Formats 1 and 2 represent 2 extremes; for format 1, all the hardware is in the carry generator, for format 2, the costs of the generalized half-adder and carry generator are roughly equal.

7. The General Theory for all Formats

The information loss chart of section 2 involves little more than simple bookkeeping. All digit sets are type a, with diminished cardinality $\delta = 1$. The weighted sum of the a's is the diminished cardinality of the structure, and remains invariant. The unweighted sum of the a's is the information content. Since the only structure used is the full adder $2a+a \leftarrow a+a+a$, which transforms three type a digit sets of weight 2^k into two type a digit sets, one of weight 2^{k+1} and one of weight 2^k, the use of a full adder results in the loss of one bit of information, and the total information loss of the structure is the number of adders used.

The generalized theory for formats 2 through 9 also involves simple bookkeeping, but is more complex because type b digit sets, as well as type a, must be included, and because three types of structures are used in the decomposition process. The type b digit set is arbitrarily assumed to require two bits of information, consistent with conventional binary logical design requirements, and conveniently equal to its diminished cardinality. For the information loss chart, it is necessary to list the number of both type b and type a digit sets of each weight, and to count the number of a's, designated by α and to count the number of b's, designated by β. These measures are redundant, since $\lambda = 2\beta+\alpha$. The information loss charts for the three elementary structures are given in Table 5.

	2^{k+1}		2^k		2^{k+1}		2^k		2^{k+1}		2^k	
	b	a	b	a	b	a	b	a	b	a	b	a
input	0	0	1	1	0	0	0	2	0	0	1	0
output	0	1	0	1	0	0	1	0	0	0	0	2
	a) carry generator				b) generalized half-adder				c) converter			

Table 5. Information Loss Chart for the Three Structural Types

The specifications of a complex structure indicate the information content, the number of type b digit sets, and the number of type a digit sets at the input and at the output. These are designated respectively as λ_{in}, β_{in}, α_{in} and λ_{out}, β_{out}, and α_{out}. From these parameters, the number of elementary structures necessary may be partially determined. Consider Table 6, in which $\Delta\lambda = \lambda_{in}-\lambda_{out}$, $\Delta\beta = \beta_{in}-\beta_{out}$, and $\Delta\alpha = \alpha_{in}-\alpha_{out}$.

	No.	λ_{in}	λ_{out}	α_{in}	α_{out}	β_{in}	β_{out}	$\Delta\lambda$	$\Delta\alpha$	$\Delta\beta$
a+a←b	x	2	2	0	2	1	0	0	-2	1
b←a+a	y	2	2	2	0	0	1	0	2	-1
2a+a←b+a	z	3	2	1	2	1	0	1	-1	1

Table 6. Analysis of the Fundamental Structural Types

If a complex structure requires x converters, y generalized half adders, and z carry generators, then for the complex structure $\Delta\lambda = z$, $\Delta\beta = z-(y-x)$ and $\Delta\alpha = 2(y-x)-z$. Since $\Delta\lambda$, $\Delta\beta$, and $\Delta\alpha$ are known, the equations may be solved to the following extent:

$$z = \Delta\lambda$$
$$y-x = \Delta\lambda-\Delta\beta$$
$$y-x = 1/2(\Delta\lambda+\Delta\alpha)$$

Thus, only the difference y-x can be determined, which is not surprising, since the converter and generalized half adder perform inverse operations.

Limited design experience indicates that the relative numbers of the elementary structures needed are roughly as follows:

1) Conversion from redundant to conventional form with all outputs type a and all inputs type b with one type a mythical input: x=y=0, all structures are carry generators.
2) All outputs type a, all inputs type a: x=0 y=z
3) All outputs type b, all inputs type b: (y-x) = 1/2z. Usually, one or two converters are necessary to make possible the use of carry generators. Each converter must be compensated for by a generalized half adder, and there appears to be a limited tradeoff between increasing the hardware requirements and decreasing the speed of operation.

8. Design of a Radix 4 Signed Digit Adder

The structure of one digital position of a radix 4 signed digit adder is shown in Figure 2. The design objective

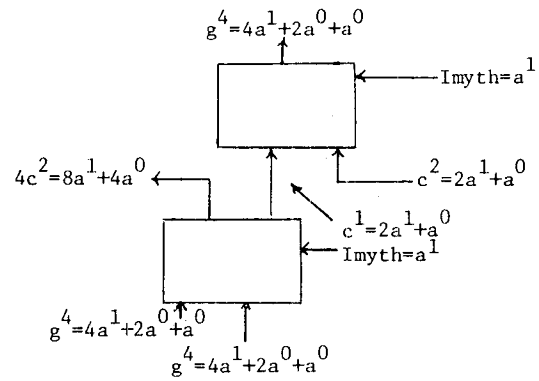

Fig. 2. Radix 4 Signed Digit Adder

is to reduce two input digit sets of type $f^3 = \{\bar{3},\bar{2},\bar{1},0,1,2,3\}$ to a single output digit set of the same type. Since $f^3 = 2b^1+b^1$ requires 4 bits for storage, the digit set $g^4 = 4a^1+2a^0+a^0$, which requires 3 bits, is used instead. The sum input $c^1 = 2a^0+a^1 = \{\bar{1},0,1,2\}$ and transfer input $c^2 = 2a^1+a^0 = \{\bar{2},\bar{1},0,1\}$ to the upper level insure that the value -4 cannot occur at the output. A mythical input a^1 is necessary for the output level in order that it will be decomposable. The input level is $4c^2+c^1 \leftarrow g^4+g^4+a^1$, where a^1 is a mythical input. For the input level, which may also be expressed as $8a^1+4a^0+2a^0+a^1 = 4a^1+4a^1+2a^0+2a^0+a^0+a^0+a^1$, $\Delta\lambda=\lambda_{in}-\lambda_{out}=7-4=3$, $\Delta\beta=0$, and $\Delta\alpha=3$, so z=3 carry generators, y-x=3. With x=0, 3 generalized half adders are required. The mythical input a^1 reduces the complexity of one of the carry generators to a single OR gate for format 2.

The output level performs the transformation $g^4 \leftarrow c^1+c^2+a^1$, or $4a^1+2a^0+a^0 \leftarrow 2a^1+2a^0+a^1+a^0+a^1$, with a^1 a mythical input. For this level $\Delta\lambda = 5-3 = 2$, $\Delta\beta=0$, and $\Delta\alpha=2$. Since x=0, 2 carry generators and two generalized half adders are needed, with simplifications possible because of the mythical input a^1. The design for both levels is summarized by Table 7.

			8		4		2		1		
LEVEL		$\lambda\beta\alpha$	b	a	b	a	b	a	b	a	Step No
INPUT	Input	707				2^2		2^0		3^1	0
	b←a+a	731			1^2		1^0		1^0	1^1	1
	$2a^0+a^1 \leftarrow b^0+a^1$	622			1^2		1^0	1^0		1^1	2
	$2a^0+a^0 \leftarrow b^0+b^0$	513			1^2	1^0		1^0		1^1	3
	$2a^1+a^0 \leftarrow b^2+a^0$	404		1^1		1^0		1^0		1^1	4
OUTPUT	Input	404						2^1		2^1	
	Myth Input	101								1^1	
	Decomp Input	505						2^1		3^2	
$b^1 \leftarrow a^0+a^1$		521					1^1		1^1	1^1	5
$2a^1+a^0 \leftarrow b^1+a^1$		412					1^1	1^1		1^0	6
$2a^1+a^0 \leftarrow b^1+a^1$		303				1^1		1^0		1^0	7

Table 7. Modified signed digit adder for radix 4

Cost factors: x = 0 y = z = 5 Mythical inputs $a^1 + a^1$.

9. Comparison with Logical Design

For the logical design of the output level of the signed digit adder of section 8, let $c^1 = 2a^0 + a^1$ be represented by w and x, let $c^2 = 2a^1 + a^0$ be represented by y and z, let the mythical input a^1 be m, and let the output $g^4 = 4a^1 + 2a^0 + a^0$ be represented by s, t, and u. From table 7, the structure is two full subtracters in cascade, since $b^1 \leftarrow a^0 + a^1$ and $2a^1 + a^0 \leftarrow b^1 + a^1$ can be combined to form $2a^1 + a^0 \leftarrow a^0 + a^1 + a^1$ in both digital positions of weights 1 and 2, as shown in Figure 3.

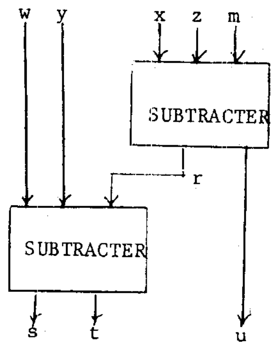

Fig. 3. Structure of Upper Level of Table 7.

From the known design expressions for a subtracter, the logical equations are

$$4 = x\overline{z} \vee m(\overline{x \vee z}) = x\overline{z}$$
$$u = x \oplus z \oplus m = x \oplus z$$
$$s = \overline{w}y \vee r(\overline{w} \vee y)$$
$$t = w \oplus y \oplus r$$

The simplifications of the expressions for r and u are due to the fact that the mythical input m is always zero.

The conventional logical design is summarized in Figure 4, and leads to the equations:

$$s = \overline{w}y \vee xy\overline{z} \vee \overline{x}\overline{w}z$$
$$t = x(w \oplus y) \vee x(\overline{w \oplus y \oplus z})$$
$$u = x \oplus z$$

which are equivalent after substitution to eliminate r. Note that the procedures of table 7 are not only much simpler than the logical design, but that they also indicate the internal structure for the design.

2	$\bar{1}$	2	$\bar{1}$		$\bar{4}$	2	1
w	x	y	z	c^1+c^2	s	t	u
0	0	0	0	0	0	0	0
0	0	0	1	1	0	0	1
0	0	1	0	$\bar{2}$	1	1	0
0	0	1	1	$\bar{1}$	1	1	1
0	1	0	0	$\bar{1}$	1	1	1
0	1	0	1	0	0	0	0
0	1	1	0	$\bar{3}$	1	0	1
0	1	1	1	$\bar{2}$	1	1	0
1	0	0	0	2	0	1	0
1	0	0	1	3	0	1	1
1	0	1	0	0	0	0	0
1	0	1	1	1	0	0	1
1	1	0	0	1	0	0	1
1	1	0	1	2	0	1	0
1	1	1	0	$\bar{1}$	1	1	1
1	1	1	1	0	0	0	0

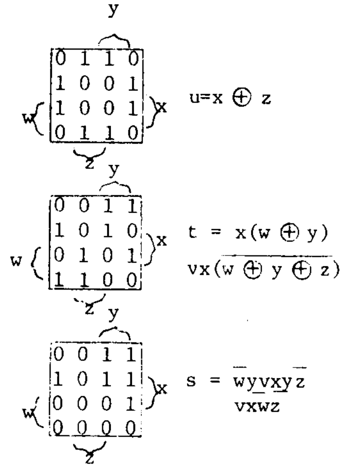

Fig. 4. Logical Design of the Output Level of Table 7

10. Example of a Signed Digit Adder for Radix 16, $\delta_d = 20$.

A useful digit set for redundant radix 16 arithmetic is the digit set with $\delta_d = 20$ and $\omega_d = 1/2\ \delta_d = 10$. As in the previous example, it is desirable to minimize the storage requirements for the digit set. The digit set $w^{11} \leftarrow 8b^1 + 4a^0 + 2a^1 + a^1$, with the capability of $\delta = 23$, is employed, and the design is such that the values $\overline{11}$, 11, and 12 of the sum cannot occur. The signed digit adder has two levels. For the input level

$16\ b^1 + r^9 \leftarrow w^{11} + w^{11} + d^3$, where d^3 is a mythical input.

For the output level

$w^{11} \leftarrow r^9 + b^1 + c^1$, where c^1 is a mythical input.

For the detailed design:

Operands and sum $w^{11} \leftarrow 8b^1 + 4a^0 + 2a^1 + a^1$

Transfer $b^1 \leftarrow a^0 + a^1$

Common digit $r^9 \leftarrow 8a^0 + 4a^1 + 2b^2 + b^1$

Mythical input $d^3 \leftarrow 2a^1 + b^1$

Mythical input $c^1 \leftarrow 2a^0 + a^1$

The design is presented in the information loss chart of table 8.

Level		λ	β	α	16 b	16 a	8 b	8 a	4 b	4 a	2 b	2 a	1 b	1 a	Step No
	Input	10	2	6			2^2			2^0		2^2		2^2	
	Myth. Input	3	1	1								1^1	1^1		
	Decomp. Input	13	3	7			2^2			2^0		3^3	1^1	2^2	0
	$2a^1+a^0 \leftarrow b^1+a^1$	12	2	8			2^2			2^0		4^4		2^1	1a
	$b^2 \leftarrow a^1+a^1$	12	3	6			2^2			2^0	1^2	2^2		2^1	1b
	$b^0 \leftarrow a^0+a^0$	12	4	4			2^2		1^0		1^2	2^2		2^1	1c
	$2a^1+a^1 \leftarrow b^2+a^1$	11	3	5			2^2		1^0	1^1		2^2		2^1	2a
Input Level	$b^1 \leftarrow a^1+a^0$	11	4	3			2^2		1^0	1^1		2^2	1^1		2b
	$2a^0+a^1 \leftarrow b^0+a^1$	10	3	4			2^2	1^0		1^1		2^2	1^1		3a
	$b^2 \leftarrow a^1+a^1$	10	4	2			2^2	1^0		1^1	1^2		1^1		3b
	$2a^0+a^1 \leftarrow b^1+a^0$	9	3	3		1^0	1^1	1^1		1^1	1^2		1^1		4
	$2a^1+a^0 \leftarrow b^1+a^1$	8	2	4		2^1		1^0		1^1	1^2		1^1		5
	Input	8	2	4				1^0		1^1	1^2		1^1	2^1	
	Myth. Input	2	0	2								1^0		1^1	
	Decomp. Input	10	2	6				1^0		1^1	1^2	1^0	1^1	3^2	5
	$2a+a \leftarrow b+a$	8	0	8				1^0		2^2		2^1		3^1	6
Output Level	$b \leftarrow a+a$	8	3	2				1^0	1^2		1^1		1^0	1^1	7
	$2a^0+a^1 \leftarrow b^0+a^1$	7	2	3				1^0	1^2		1^1	1^0		1^1	8
	$2a^0+a^1 \leftarrow b^1+a^0$	6	1	4				1^0	1^2	1^0		1^1		1^1	9
	$2a^1+a^0 \leftarrow b^2+a^0$	5	0	5				2^1		1^0		1^1		1^1	10
	$b^1 \leftarrow a^1+a^0$	5	1	3			1^1			1^0		1^1		1^1	11

Cost Factors a) Input Level: x=0 y=4 z=5
Myth Input = $2a^1+b^1$ b) Output Level: x=0 y=4 z=5
Myth Input = $2a^0+a^1$

Table 8. Information Loss Chart for Radix 16 Signed-Digit Adder with $\delta_d=20$

The purpose of the example of Table 8 is to indicate the relative ease with which a complex structure may be decomposed. The total cost of the two levels of the structure is 10 carry generators and 8 generalized half adders, without taking into account the simplifications possible due to mythical inputs. The conventional logical design of the structure would have 10 binary inputs and 8 outputs for the input level, and 8 binary inputs and 5 outputs for the output level, and would give no indication of the internal connectivity.

11. Conclusions

This paper summarizes the theoretical background for a procedure for the decomposition of complex structures for binary addition and subtraction into a limited number of variants of elementary structures. The theory is presented here in terms of its simplest form, and relies on the use of two valued type a digit sets and three valued type b digit sets for binary arithmetic. An unexpected result, useful for higher radix structures (with $r=2^k$, and k an integer), is that there exists a unique representation for digit sets of higher diminished cardinality, as a weighted combination of type a and type b digit sets. For a given diminished cardinality δ, the representation is easily found by a procedure similar to decimal to binary conversion, except that remainders of 1 or 2 are found at each step. For example, if δ=49, the representation is found by the procedure of Table 9.

2	)49	
2	)24	1
2	)11	2
2	) 5	1
2	) 2	1
	0	2

Table 9. Representation of digit set with δ=49

The pattern of remainders indicates the use of a's and b's; least significant weight first, so the representation for δ=49 is 16b+8a+4a+2b+a. Designations and the corresponding unique representation for δ<32 are given in Appendix I.

Only structures of diminished cardinality 2 and 3 are considered as elementary structures here. The theory can accommodate other elementary structures, such as, for example, 2a+b←b+b, with δ=4. For brevity, little attention has been given to the use of offset. A topic for future investigation is the development, if possible, of procedures of introducing offset in a manner that will reduce the number of variants necessary.

For brevity, detailed logical designs are not included here, but are found in Reference 12.10 in the bibliography. A companion paper (Reference 12.11) extends the theory to odd radices and binary multiples of odd radices, with emphasis on radix 10.

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Designation	δ	representation	bits
a	1	a	1
b	2	b	2
c	3	2a+a	2
d	4	2a+b	3
e	5	2b+a	3
f	6	2b+b	4
g	7	4a+2a+a	3
h	8	4a+2a+b	4
i	9	4a+2b+a	4
j	10	4a+2b+b	5
k	11	4b+2a+a	4
l	12	4b+2a+b	5
m	13	4b+2b+a	5
n	14	4b+2b+b	6
o	15	8a+4a+2a+a	4
p	16	8a+4a+2a+b	5
q	17	8a+4a+2b+a	5
r	18	8a+4a+2b+b	6
s	19	8a+4b+2a+a	5
t	20	8a+4b+2a+b	6
u	21	8a+4b+2b+a	6
v	22	8a+4b+2b+b	7
w	23	8b+4a+2a+a	5
x	24	8b+4a+2a+b	6
y	25	8b+4a+2b+a	6
z	26	8b+4a+2b+b	7
A	27	8b+4b+2a+a	6
B	28	8b+4b+2a+b	7
C	29	8b+4b+2b+a	7
D	30	8b+4b+2b+b	8
E	31	16a+8a+4a+2a+a	5

Appendix I. Binary representation of Digit Sets of Higher Cardinality.

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