Foreword

The 7th Symposium on Computer Arithmetic (ARITH–7) was held at the University of Illinois in Urbana, Illinois, on June 4-6, 1985. A total of 47 papers were accepted for presentation. These papers covered theoretical foundations, arithmetic algorithms, processor architectures, hardware and software implementations, error controls and advanced applications of high-speed and high-accuracy arithmetic systems in modern digital computers. This year's symposium is divided into 11 technical sessions. The sessions include efficient adders and ALU designs, fast multipliers and dividers, floating-point arithmetic, systolic arithmetic schemas, directions in computer arithmetic, elementary function evaluation, rational and residue arithmetic, signal and image processing, large-scale scientific computations, fault-tolerant arithmetic, and new arithmetic systems.

Contributions to this Proceedings were made by 82 authors from almost all parts of the world. However, the majority of the papers received were from North America. All the previous symposia on computer arithmetic were held in the U.S.; however, ARITH–6 was held in Aarhus, Denmark in 1983. The interval between successive meetings in the series has been reduced from three years to two years in the last three meetings (1981, 1983, and 1985). This prompts us to suggest that the future symposia will be held alternately between North America and other continents every two-year period.

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Despain, Alvin	Matula, David	Tu, Paul
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Fisher, P.D.	Ong, Shauchi	Wakerly, John F.
Flynn, Michael J.	Osteeby, Ole	Woo, Bob Y.
Garner, Harvey L.	Piestrak, Stanislaw	Xu, Zhiwei

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