A MULTIOPERAND TWO'S COMPLEMENT ADDITION ALGORITHM

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ABSTRACT

This paper presents a novel algorithm for summing a set of 2's complement numbers in parallel. The 2's complement addition is converted to an equivalent parallel summation of unsigned numbers. The conversion is performed by simply complementing all the sign bits. Only a few constant bits are required for sign correction. This algorithm is suitable for computer-aided design (CAD) of custom VLSI.

INTRODUCTION

Multioperand addition is essential in parallel convolution necessary for real-time signal and image processing [1]. Baugh and Wooley's algorithm [2] allows unsigned implementation techniqes for parallel multiplication. However, a set of signed product terms generated by these multipliers needs to be summed in parallel.

This paper describes a parallel algorithm for adding a set of 2's complement numbers. Carry-save adder (CSA) networks synthesized by a CAD tool [3] are used as implementation examples.

ALGORITHM

The sum S of M n-bit 2's complemnt numbers is expressed as:

$$S = \sum_{k=1}^{M} \left[- x_{(n-1)k}\, 2^{n-1} + \sum_{i=0}^{n-2} x_{ik}\, 2^{i} \right]$$

$$= - \sum_{k=1}^{M} x_{(n-1)k}\, 2^{n-1} + \sum_{k=1}^{M} \sum_{i=0}^{n-2} x_{ik}\, 2^{i} \qquad (1)$$

where $x_{(n-1)k}$ is the sign bit and x_{ik} is the i-th significant bit of the k-th operand. The negative term in (1) is replaced by

$$\sum_{k=1}^{M} \bar{x}_{(n-1)k}\, 2^{n-1} - M\, 2^{n-1}$$

where $\bar{x}_{(n-1)k}$ is the complement of the sign bit. Eq. (1) is then rewritten as:

$$S = \sum_{k=1}^{M} \bar{x}_{(n-k)k}\, 2^{n-1} + \sum_{k=1}^{M} \sum_{i=0}^{n-2} x_{ik}\, 2^{i}$$

$$- M\, 2^{n-1} \qquad (2)$$

where the negative term depends on only the number M of operands.

The following two cases of M-operand addition are considered. CSA networks are used as implemetnation examples.

Case A: M is the d-th power of 2, where d is an integer. The negative term in (2) is only the (n-1+d)th power of 2. Figure 1 shows a CSA network [3] for M = 8 and n = 8, where "o's" are positive bits and "●'s" are complemented sign bits. Note that all summand bits are positive allowing unsigned implementation techniques for parallel addition. The sum is obtained by simply complementing the most significant bit (MSB).

Case B: M is not the d-th power of 2. The negative term in (2) is:

$$\sum_{r=0}^{d-1} \bar{m}_r\, 2^{n-1+r} + 2^{n-1} - 2^{n-1+d} \qquad (3)$$

Figure 2 shows a CSA network for M = 5 and n = 8, where "1's" are constant bits for sign correction. The sum is obtained by simply complementing the MSB.

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CONCLUSION

A new algorithm for parallel two's complement addition has been presented. The complexity of parallel 2's complement adders is significantly reduced by simply complementing all the sign bits. This approach is applicable for CAD of custom VLSI.

REFERENCES

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2. C. R. Baugh and B. A. Wooley, "A Two's Complement Parallel Array Multiplication Algorithm," IEEE Trans. Comput., vol. C-22, pp. 1045-1047, Dec. 1973.

3. H. Kobayashi and T. A. Smith, "SPAN: A Synthesis Program for Adder Networks," 1st Int. Conf. Computers and Applications, Beijing, China, June 1984, pp. 710-714.

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                   SPAN V1.00

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   ---------------------------------
               ●   o   o   o   o   o   o   o
               ●   o   o   o   o   o   o   o
               ●   o   o   o   o   o   o   o
               ●   o   o   o   o   o   o   o
               ●   o   o   o   o   o   o   o
               ●   o   o   o   o   o   o   o
               ●   o   o   o   o   o   o   o
               ●   o   o   o   o   o   o   o
   --------------------------------- 14-FA  1-HA
           o   o   o   o   o   o   o   o   o
           o   o   o   o   o   o   o   o   o
               o   o   o   o   o   o   o   o
               o   o   o   o   o   o   o   o
               o   o   o   o   o   o   o   o
               o   o   o   o   o   o   o   o
   --------------------------------- 14-FA  1-HA
           o   o   o   o   o   o   o   o   o
           o   o   o   o   o   o   o   o   o
           o   o   o   o   o   o   o   o   o
           o   o   o   o   o   o   o   o   o
   ---------------------------------  8-FA  1-HA
       o   o   o   o   o   o   o   o   o   o
           o   o   o   o   o   o   o   o   o
           o   o   o   o   o   o   o   o   o
   ---------------------------------  8-FA  1-HA
       o   o   o   o   o   o   o   o   o   o
       o   o   o   o   o   o   o   o   o   o
   ---------------------------------  CLA
   ●   o   o   o   o   o   o   o   o   o   o
  10   9   8   7   6   5   4   3   2   1   0

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              Stages           4
              FAs             44
              HAs              4
              Gates          368
              CLA             10
              CPU Time (ms)  230

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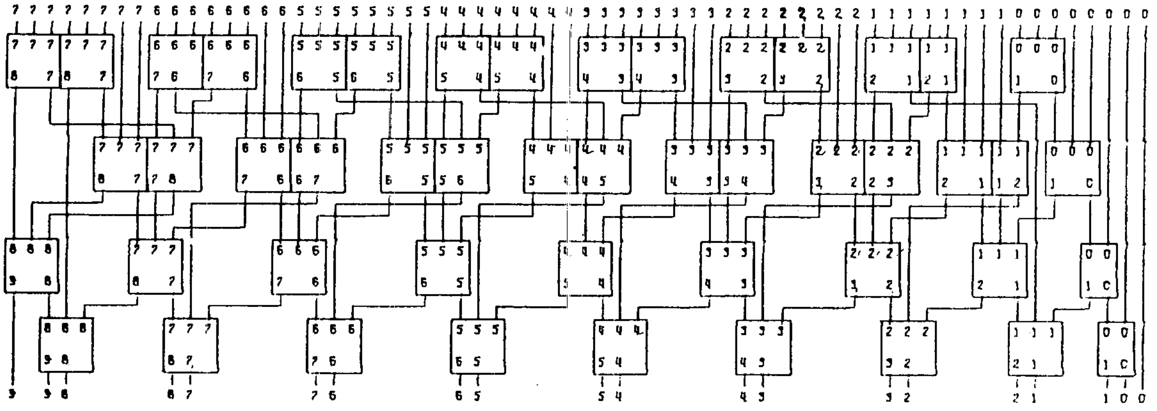
(a)



(b)

Figure 1. CSA network for M = 8 and n = 8. (a) Logic synthesis. (b) Circuit layout.

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   ---------------------------------
          1  ●  o  o  o  o  o  o  o
             ●  o  o  o  o  o  o  o
             ●  o  o  o  o  o  o  o
             ●  o  o  o  o  o  o  o
             ●  o  o  o  o  o  o  o
             1
   ---------------------------------  7-FA  2-HA
          o  o  o  o  o  o  o  o  o
          o  o  o  o  o  o  o  o  o
          o  o  o  o  o  o  o  o  o
             o  o  o  o  o  o  o  o
   ---------------------------------  7-FA  2-HA
       o  o  o  o  o  o  o  o  o  o
          o  o  o  o  o  o  o  o  o
          o  o  o  o  o  o  o  o  o
   ---------------------------------  8-FA  1-HA
       o  o  o  o  o  o  o  o  o  o
       o  o  o  o  o  o  o  o  o  o
   ---------------------------------  CLA
    ●  o  o  o  o  o  o  o  o  o  o
   10  9  8  7  6  5  4  3  2  1  0

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             Stages            3
             FAs              22
             HAs               5
             Gates           196
             CLA              10
             CPU Time (ms)   140

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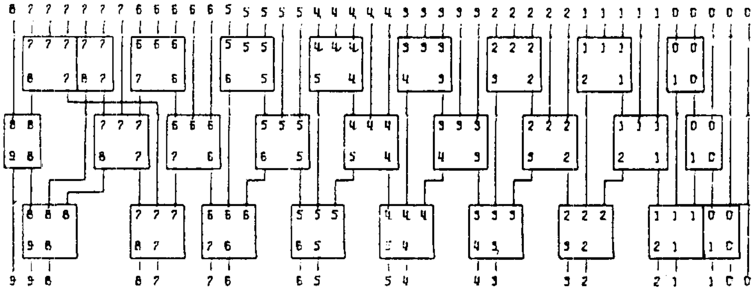
```

(a)



(b)

Figure 2. CSA network for M = 5 and n = 8. (a) Logic synthesis.
(b) Circuit layout.